

N-Channel 100 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
100	5.2 @ $V_{GS} = 10V$	80 ⁽¹⁾
	7.0 @ $V_{GS} = 4.5V$	

Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- Motor drives

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Package and ordering information

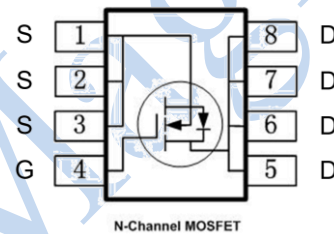
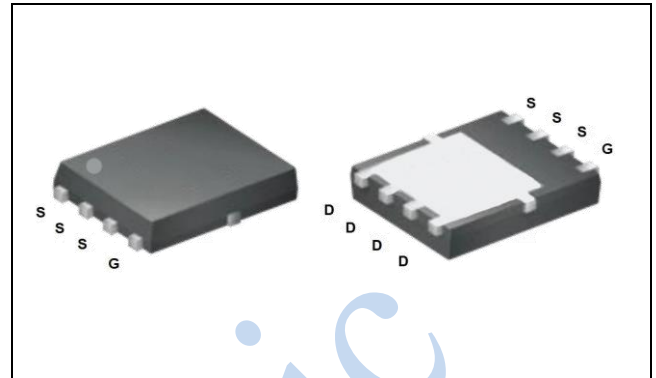
Ordering code	Package	Device code
SDN10K5P2S2C	PDFN5X6-8L	AAT

1. Maximum ratings

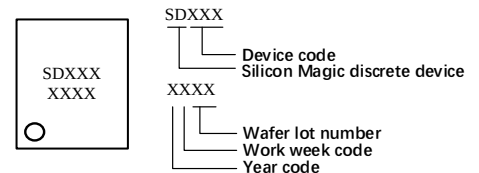
Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	100	V
Drain-source voltage spike, 10μs		V _{DS}	120	
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C ⁽¹⁾	I _D	80	A
	T _C =100°C		73	
	T _A =25°C ⁽⁴⁾		16	
Pulsed drain current ⁽²⁾		I _{D,pulse}	320	
Avalanche energy, single pulse ⁽³⁾		E _{AS}	204	mJ
Power dissipation	T _C =25°C	P _D	125	W
	T _A =25°C ⁽⁴⁾		2.7	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to 150	°C

PDFN5X6-8L



RoHS
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2. Thermal resistance ratings

Thermal resistance ratings						
Parameter		Symbol	Max.	Unit		
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	1.0	°C/W		
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	45			

3. Electrical Characteristics

Electrical characteristics (T _A = 25°C unless otherwise noted)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0, I _D = 250 μA	100			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.2	1.9	2.6	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 100 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 40 A		4.8	5.2	mΩ
		V _{GS} = 4.5 V, I _D = 16 A		6.1	7	
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 40 A		97		S
Gate resistance	R _g	f = 1MHz		1	2	Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 50 V, I _D = 40 A, V _{GS} = 10 V		56	79	nC
Gate-source charge	Q _{gs}			10	14	
Gate-drain charge	Q _{gd}			16	23	
Turn-on delay time	t _{d(on)}	V _{DS} = 50 V, I _D = 40 A, V _{GS} = 10 V, R _{GEN} = 3 Ω		16	32	ns
Rise time	t _r			22	44	
Turn-off delay time	t _{d(off)}			48	96	
Fall time	t _f			14	28	
Input capacitance	C _{iss}	V _{DS} = 50 V, V _{GS} = 0 V, f = 1 MHz		2200	3080	pF
Output capacitance	C _{oss}			415	580	
Reverse transfer capacitance	C _{rss}			15	30	
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 40 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 50 V, I _F = 40 A, di/dt = 100 A/μs		150	270	ns
Reverse recovery charge	Q _{rr}			263	475	nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 75 \text{ V}, V_{GS} = 10 \text{ V}, L = 0.3 \text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

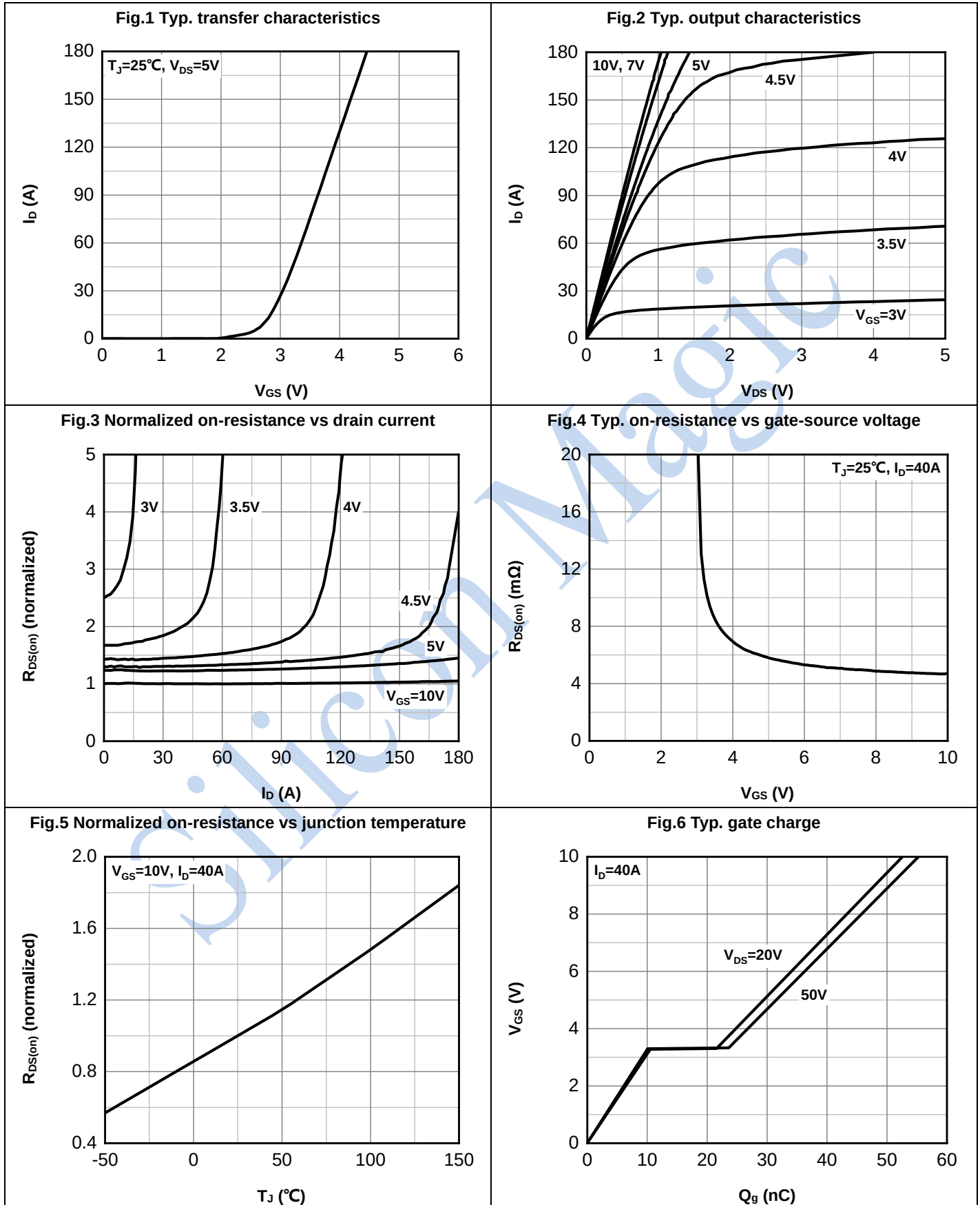


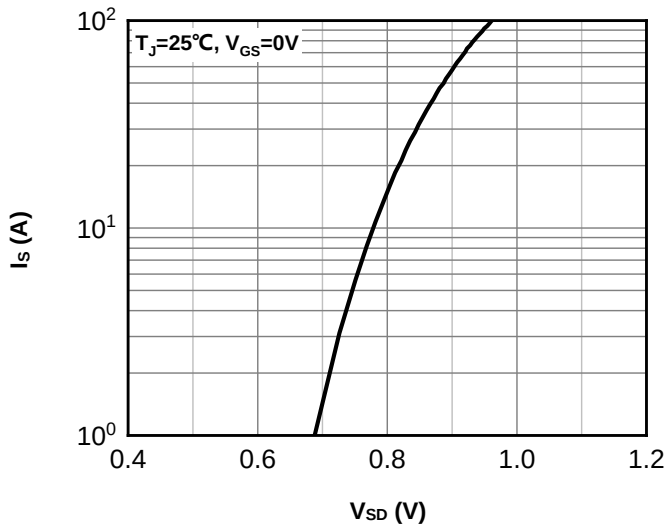
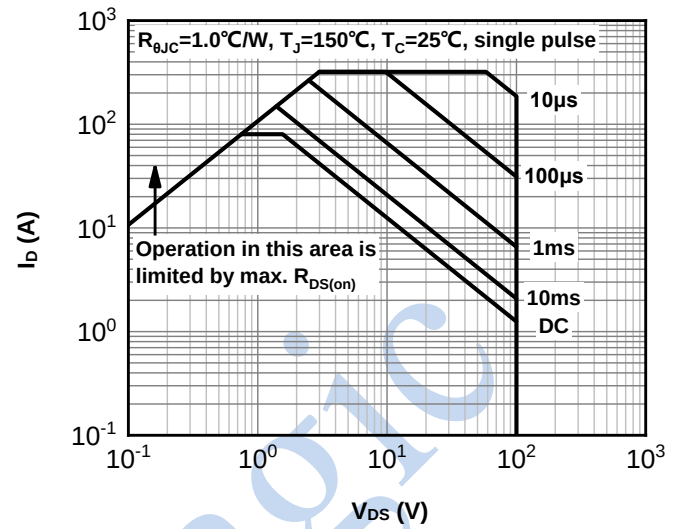
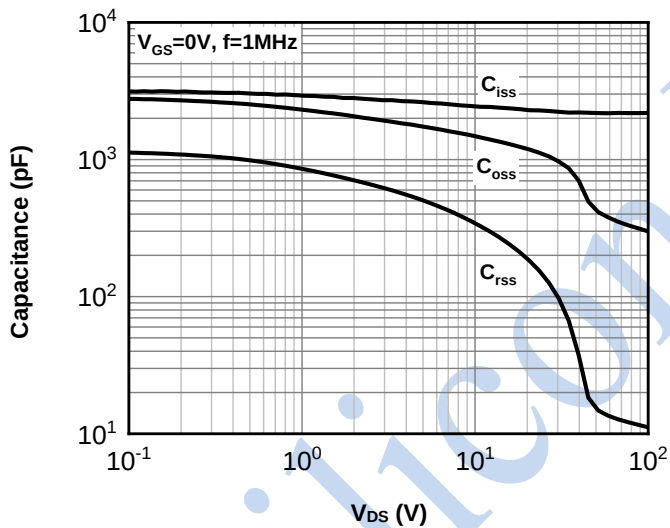
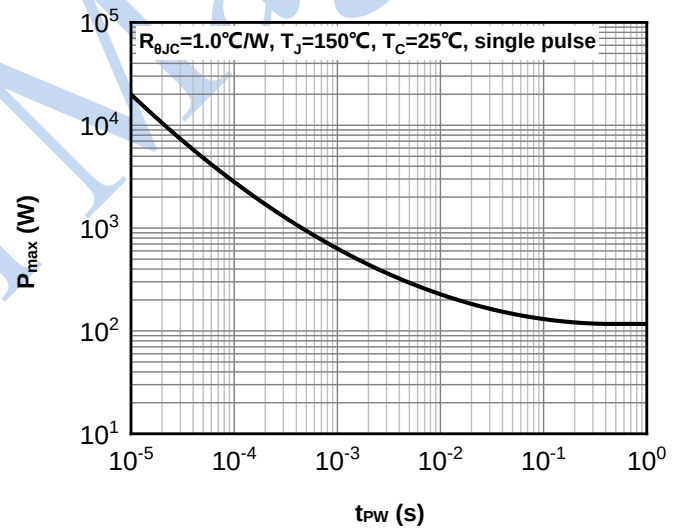
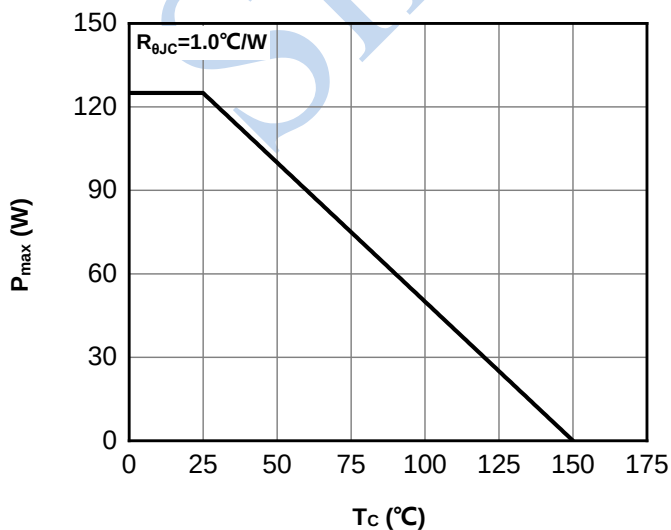
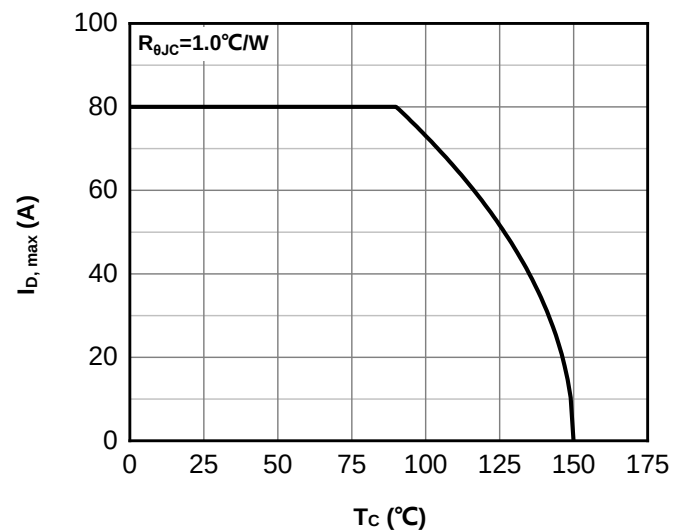
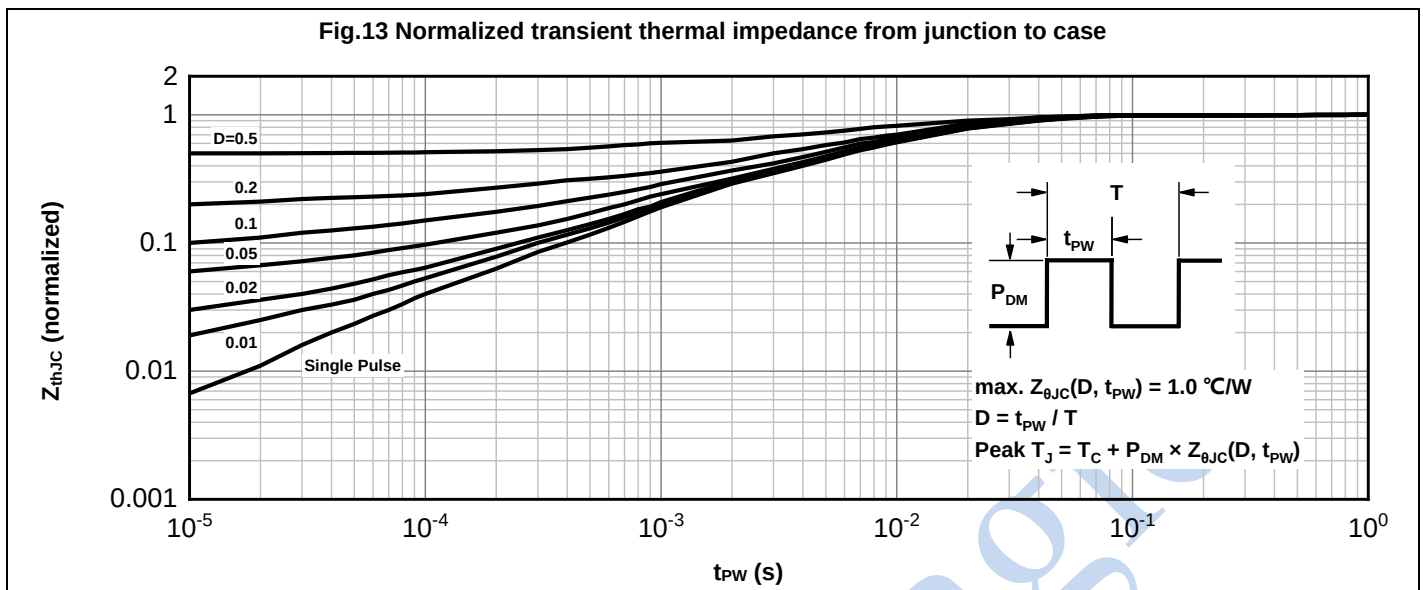
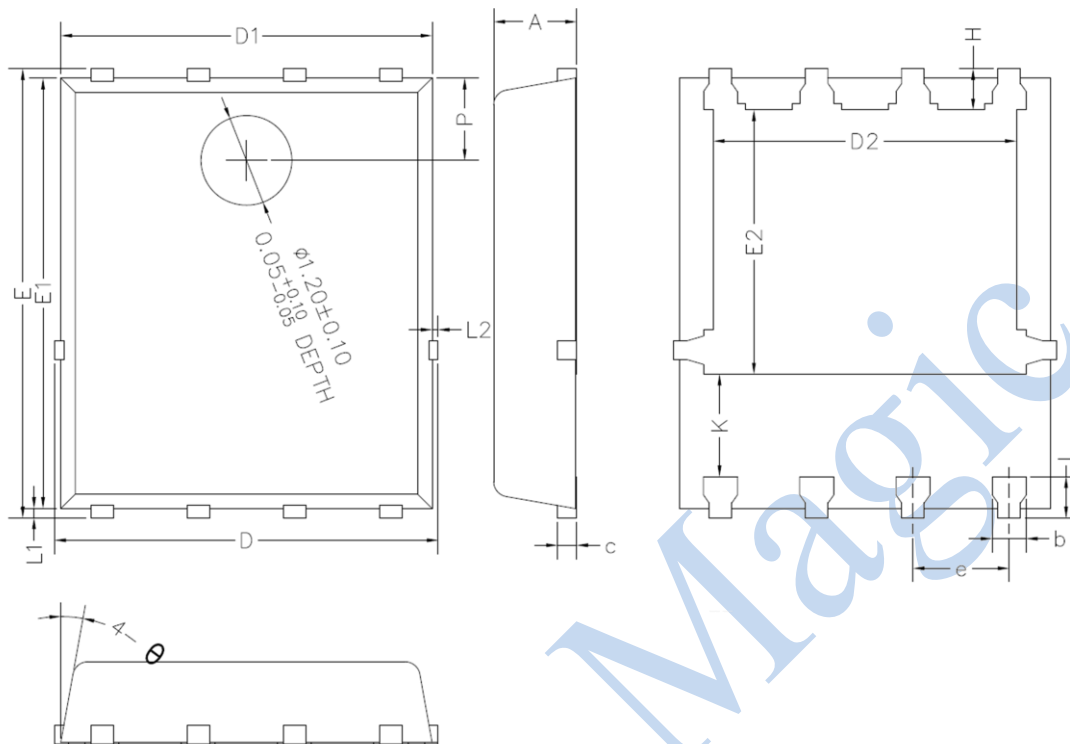
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	0.900	1.050	1.200
b	0.310	0.425	0.540
c	0.210	0.275	0.340
D	4.800	5.100	5.400
D1	4.800	4.975	5.150
D2	3.900	4.050	4.200
e	1.170	1.270	1.370
E	5.900	6.075	6.250
E1	5.500	5.650	5.800
E2	3.425	3.528	3.630
H	0.450	0.6250	0.800
K	1.125	1.348	1.570
L	0.450	0.575	0.700
L1	0.000	0.188	0.375
L2	0.000	0.075	0.150
P	1.000	1.100	1.200
θ	8°	10°	12°

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