

N-Channel 100 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
100	4.2 @ $V_{GS} = 10V$	117 ⁽¹⁾

Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

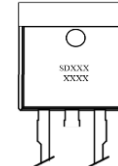
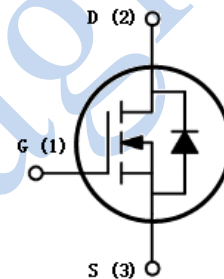
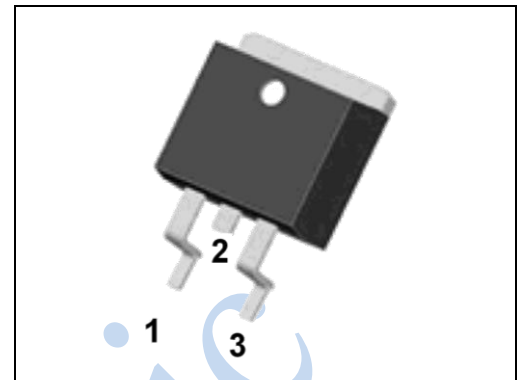
Applications

- DC/DC conversion
- Power switch
- Motor drives

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Package and ordering information

Ordering code	Package	Device code
SDN10N4P2S2B	TO263-3L	ACE

TO263-3L


SDXXX
Device code
Silicon Magic discrete device

XXXX
Wafer lot number
Work week code
Year code

1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V _{DS}	100	V
Gate-source voltage		V _{GS}	±20	
Continuous drain current	T _C =25°C ⁽¹⁾	I _D	117	A
	T _C =100°C		97	
	T _A =25°C ⁽⁴⁾		20	
Pulsed drain current ⁽²⁾		I _{D,pulse}	468	
Avalanche energy, single pulse ⁽³⁾		E _{AS}	529	mJ
Power dissipation	T _C =25°C	P _D	178	W
	T _A =25°C ⁽⁴⁾		3.1	
Operating junction and storage temperature range		T _J , T _{stg}	-55 to 150	°C

2. Thermal resistance ratings

Thermal resistance ratings						
Parameter		Symbol	Max.	Unit		
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.7	°C/W		
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	40			

3. Electrical characteristics

Electrical characteristics						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0, I_D = 250 \mu A$	100			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.2	3	3.8	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			±100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100 V, V_{GS} = 0 V$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 18 A$		3.8	4.2	mΩ
Forward transconductance ⁽⁵⁾	g_{fs}	$V_{DS} = 5 V, I_D = 18 A$		64		S
Gate resistance	R_g			1	2	Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q_g	$V_{DS} = 50 V, I_D = 18 A, V_{GS} = 10 V$		78	110	nC
Gate-source charge	Q_{gs}			17	24	
Gate-drain charge	Q_{gd}			22	31	
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 50 V, I_D = 18 A, V_{GS} = 10 V,$ $R_{GEN} = 6 \Omega$		31	62	ns
Rise time	t_r			25	50	
Turn-off delay time	$t_{d(off)}$			77	154	
Fall time	t_f			32	64	
Input capacitance	C_{iss}	$V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz$		4350	6090	pF
Output capacitance	C_{oss}			685	960	
Reverse transfer capacitance	C_{rss}			10	20	
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0 V, I_F = 18 A$		0.8	1.1	V
Reverse recovery time	t_{rr}	$V_{DS} = 50 V, I_F = 18 A, di/dt = 100 A/\mu s$		75	135	ns
Reverse recovery charge	Q_{rr}			165	297	nC

Notes

- (1) Package limited
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 75 V, V_{GS} = 10 V, L = 0.3 mH$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

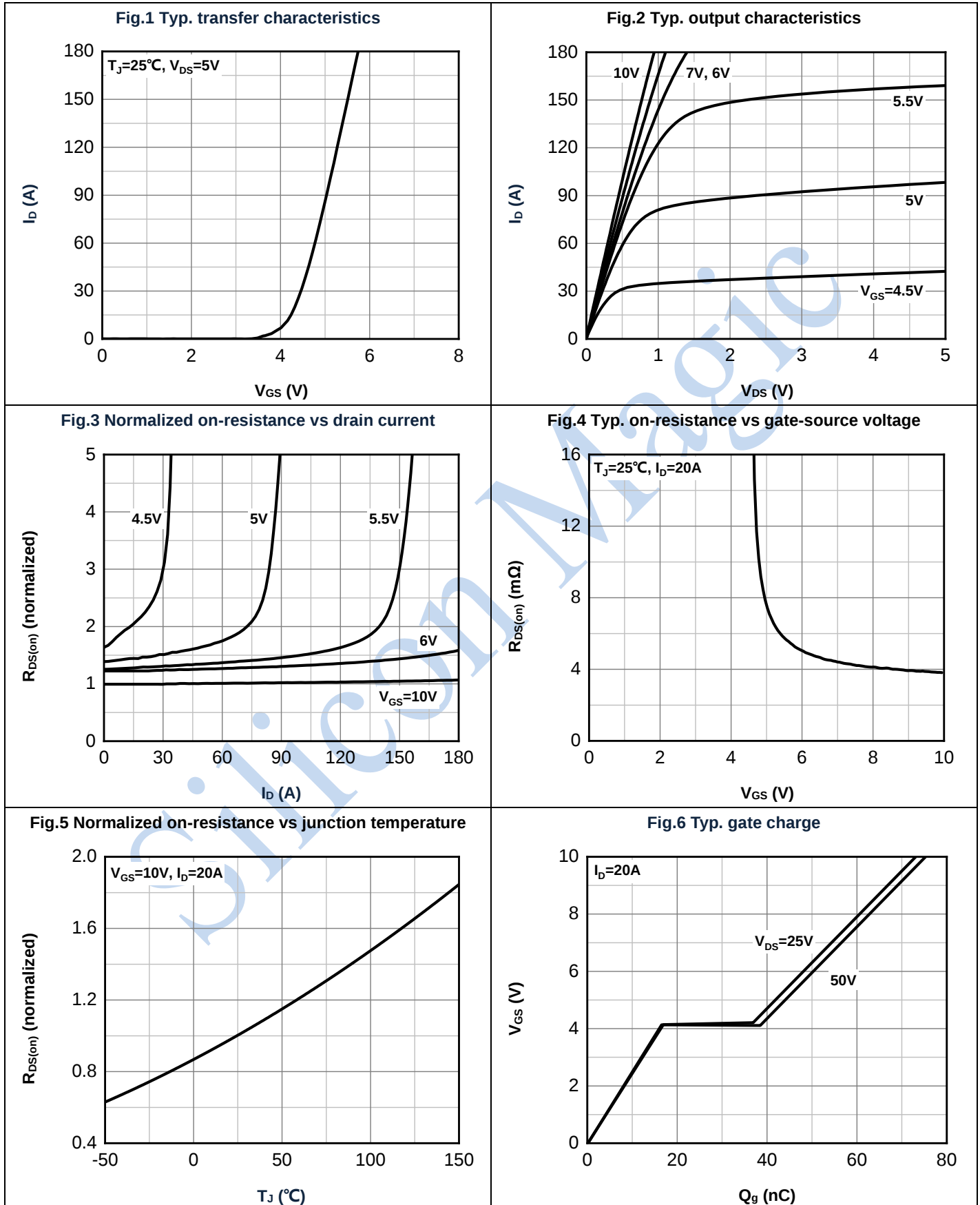


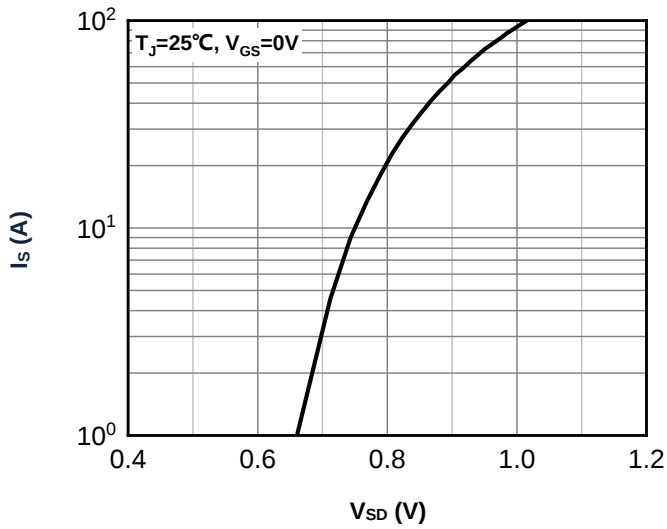
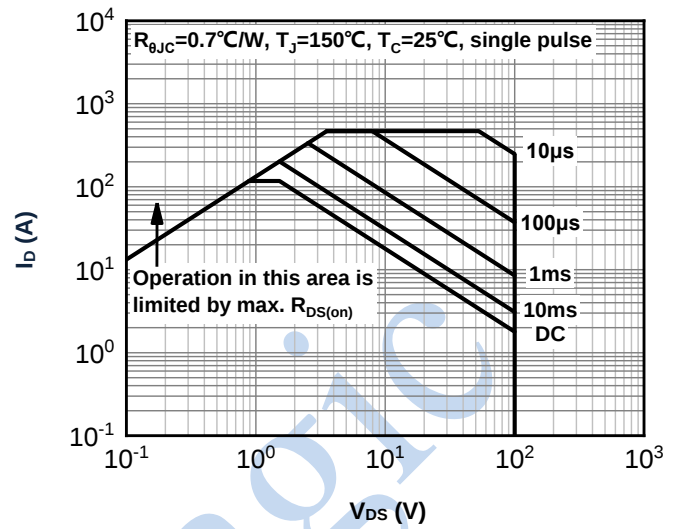
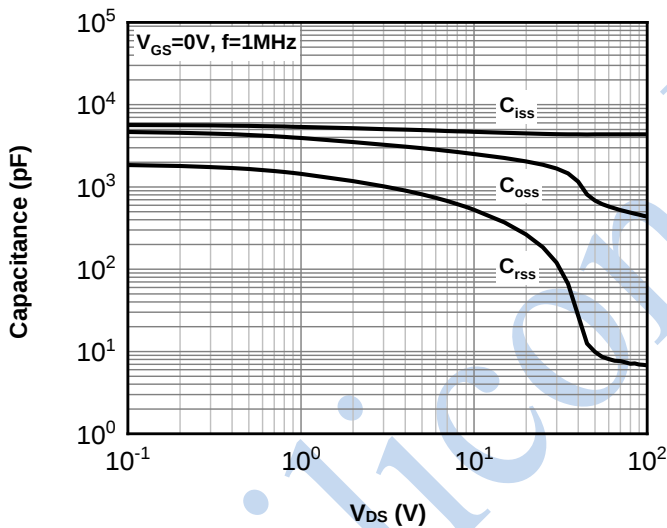
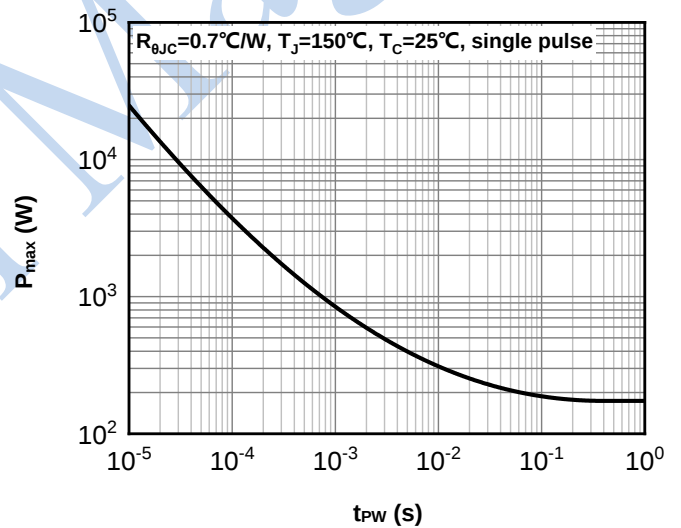
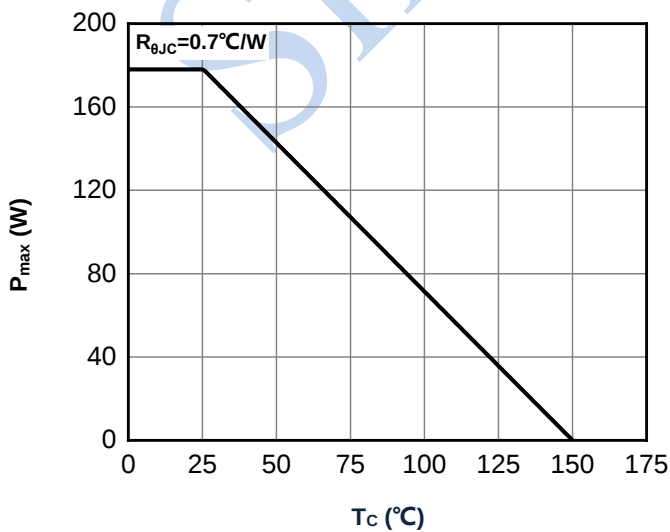
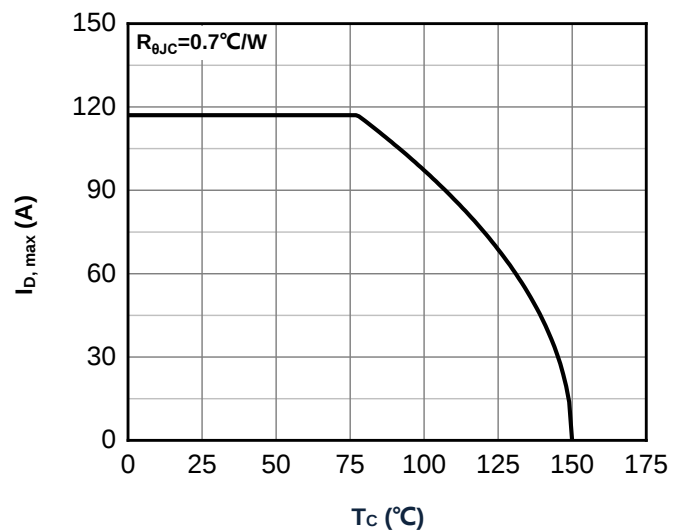
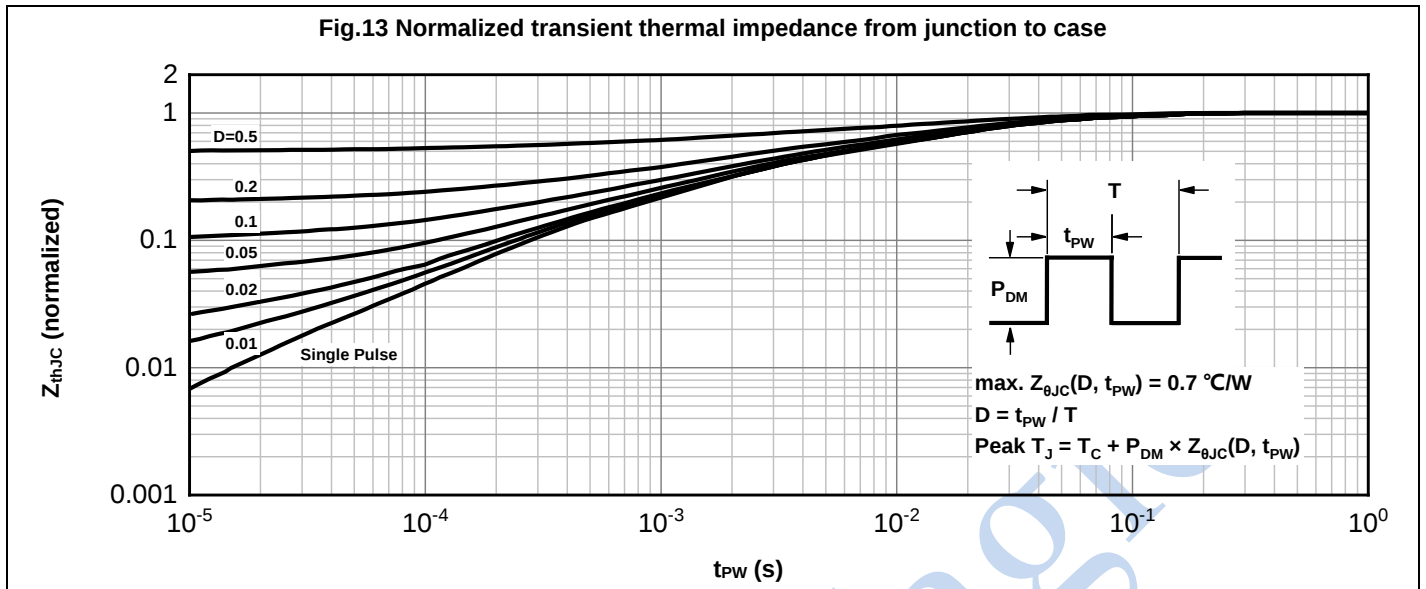
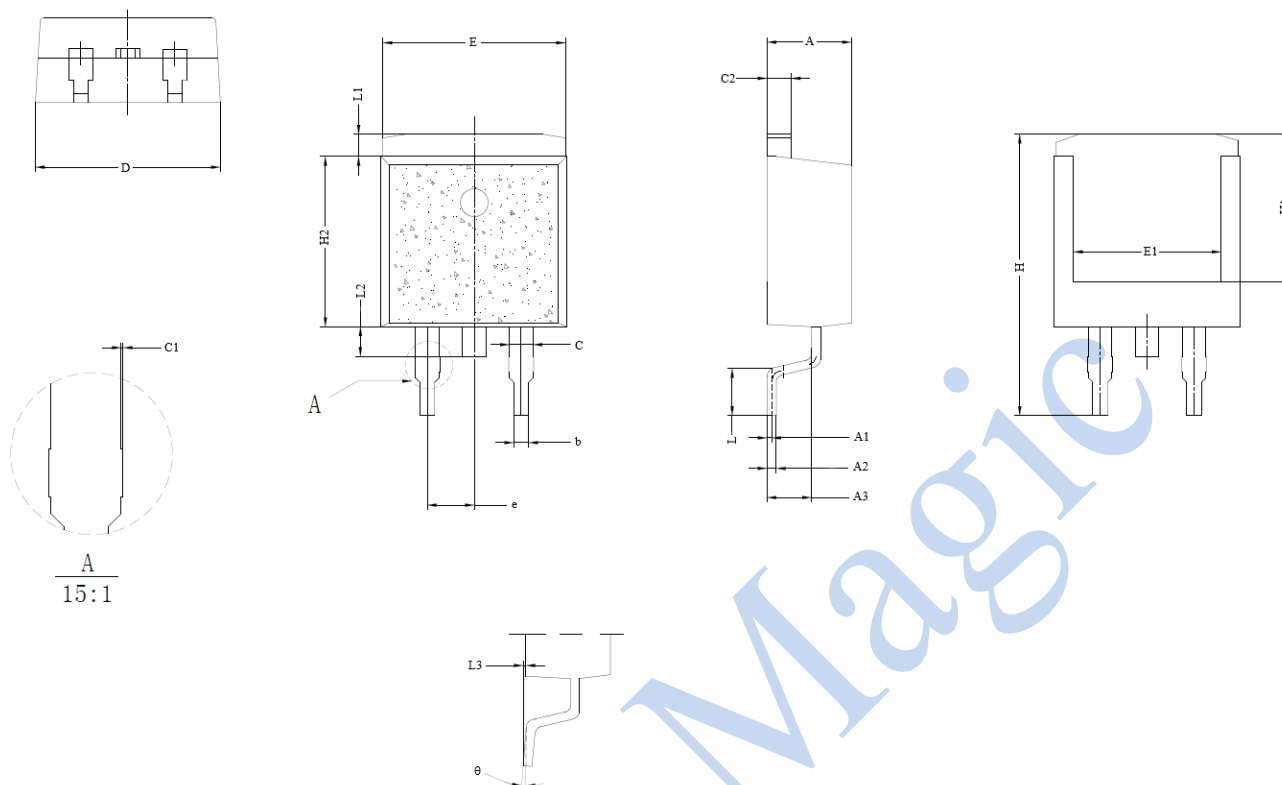
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	4.47	4.57	4.67
A1	-	0.25	-
A2	-	0.50	-
A3	2.34	2.40	2.46
b	0.70	0.80	0.90
C	1.20	1.27	1.35
C1	-	-	0.08
C2	-	1.30	-
D	9.90	10.00	10.10
E	9.78	9.88	9.98
E1	7.50	8.00	8.50
e	2.54 BSC		
H	15.00	15.40	15.80
H1	7.50	8.00	8.15
H2	9.00	9.20	9.40
L	1.70	2.00	2.30
L1	1.05	1.25	1.45
L2	1.40	1.60	1.78
L3	0.00	-	0.25
θ	0°	-	5°

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