

N-Channel 100 V MOSFET

Product summary


V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
100	2.7 @ $V_{GS} = 10V$	166 ⁽¹⁾

Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

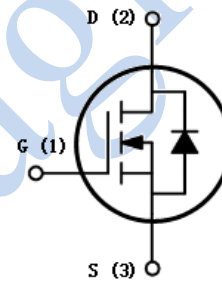
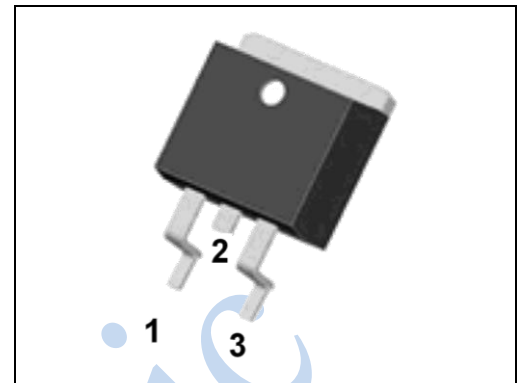
Applications

- DC/DC conversion
- Power switch
- Motor drives

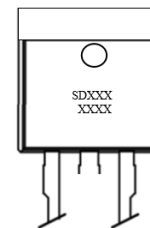
 is the registered trademark of Hangzhou Silicon-Magic Semiconductor Technology Co., Ltd.

Package and ordering information

Ordering code	Package	Device code
SDN10N2P7S2B	TO263-3L	ACA

TO263-3L


RoHS
COMPLIANT
HALOGEN
FREE



SDXXX
Device code
Silicon Magic discrete device

XXXX
Wafer lot number
Work week code
Year code

1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit	
Drain-source voltage	V_{DS}	100	V	
Gate-source voltage	V_{GS}	± 20		
Continuous drain current	I_D	$T_C=25^\circ\text{C}$ ⁽¹⁾	166	
		$T_C=100^\circ\text{C}$	143	
		$T_A=25^\circ\text{C}$ ⁽⁴⁾	25	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	664	A	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	629		mJ
Power dissipation	P_D	$T_C=25^\circ\text{C}$	250	W
		$T_A=25^\circ\text{C}$ ⁽⁴⁾	3.1	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$	

2. Thermal resistance ratings

Thermal resistance ratings				
Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.5	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	40	

3. Electrical Characteristics

Electrical characteristics						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0, I_D = 250 \mu A$	100			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.2	3	3.8	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0 V, V_{GS} = \pm 20 V$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100 V, V_{GS} = 0 V$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10 V, I_D = 25 A$		2.4	2.7	m Ω
Forward transconductance ⁽⁵⁾	g_{fs}	$V_{DS} = 5 V, I_D = 25 A$		102		S
Gate resistance	R_g			1	2	Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q_g	$V_{DS} = 50 V, I_D = 25 A, V_{GS} = 10 V$		150	210	nC
Gate-source charge	Q_{gs}			32	45	
Gate-drain charge	Q_{gd}			45	63	
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 50 V, I_D = 25 A, V_{GS} = 10 V, R_{GEN} = 6 \Omega$		46	92	ns
Rise time	t_r			48	96	
Turn-off delay time	$t_{d(off)}$			132	264	
Fall time	t_f			68	136	
Input capacitance	C_{iss}	$V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz$		8400	11760	pF
Output capacitance	C_{oss}			1150	1610	
Reverse transfer capacitance	C_{rss}			26	52	
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0 V, I_F = 25 A$		0.8	1.1	V
Reverse recovery time	t_{rr}	$V_{DS} = 50 V, I_F = 25 A, di/dt = 100 A/\mu s$		90	162	ns
Reverse recovery charge	Q_{rr}			264	476	nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 75 V, V_{GS} = 10 V, L = 0.3 mH$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

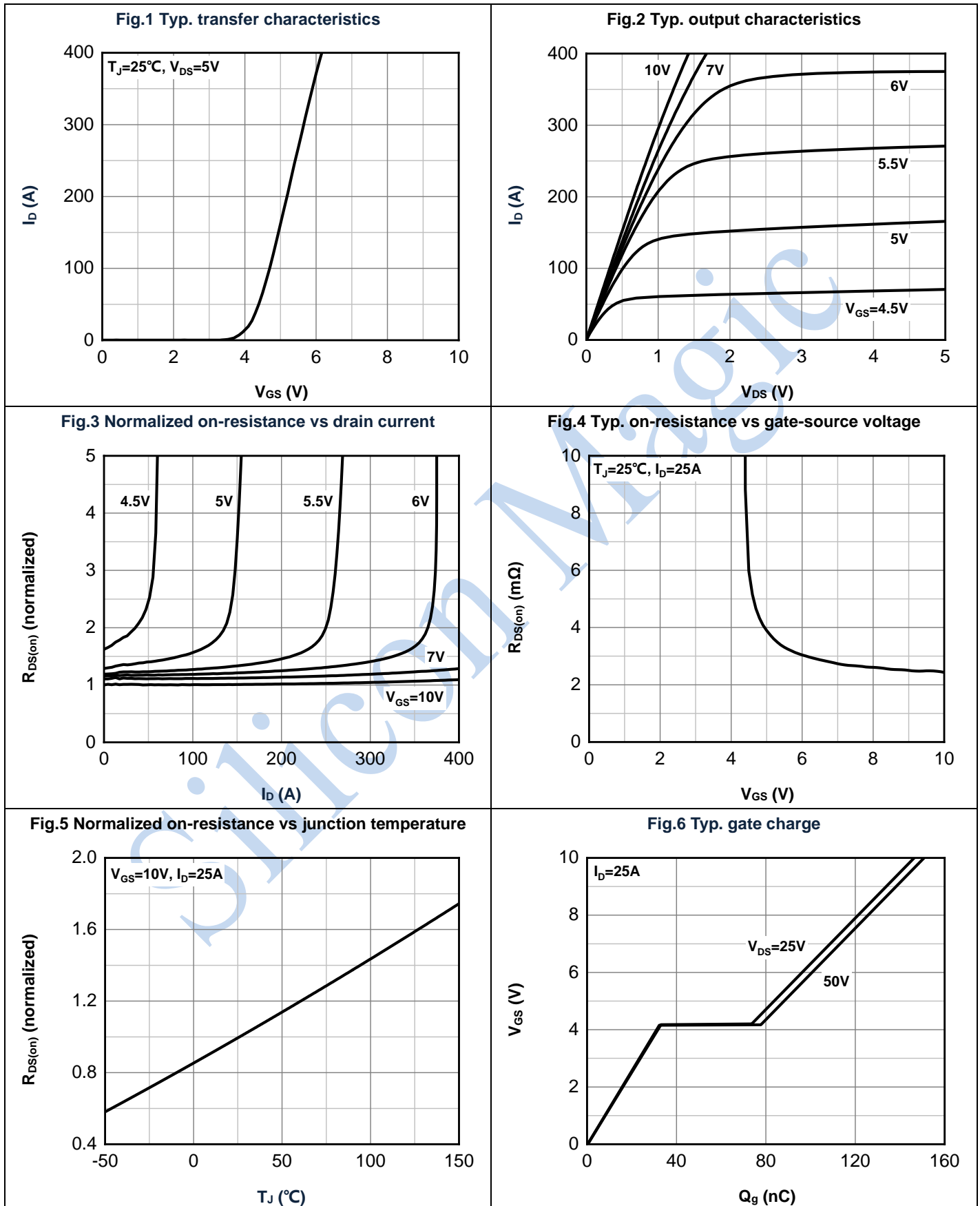


Fig.7 Typ. forward characteristics of body diode

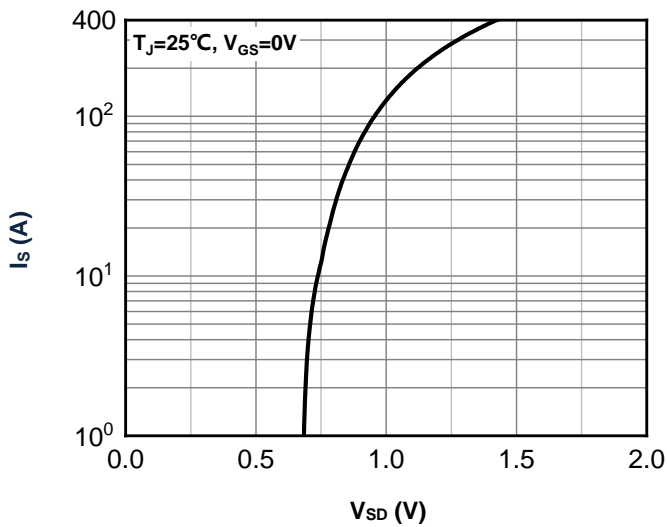


Fig.8 Safe operating area

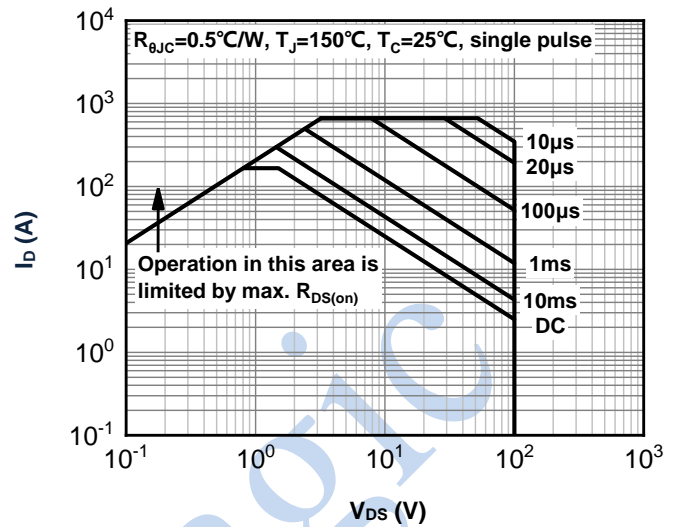


Fig.9 Typ. Capacitance

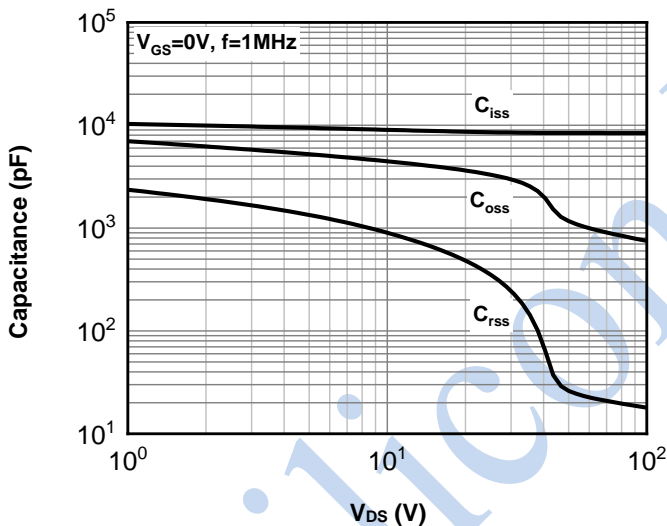


Fig.10 Single pulse maximum power dissipation

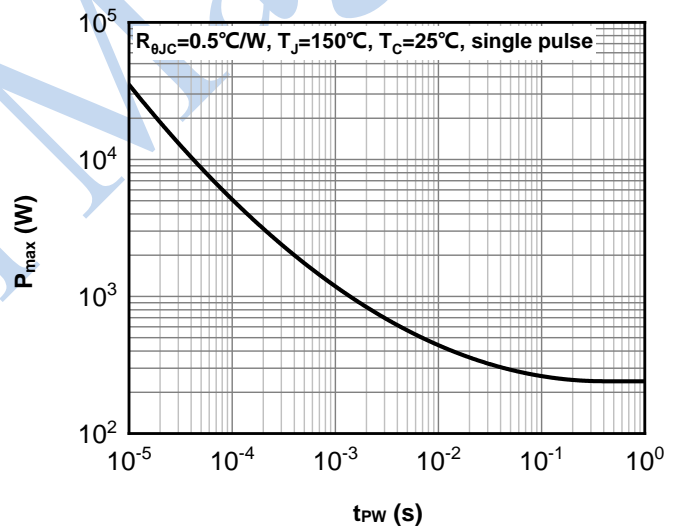


Fig.11 Max. power dissipation vs case temperature

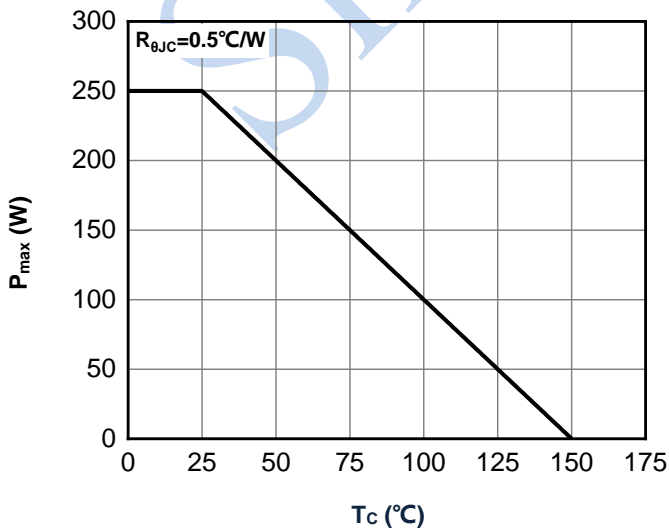


Fig.12 Max. continuous drain current vs case temperature

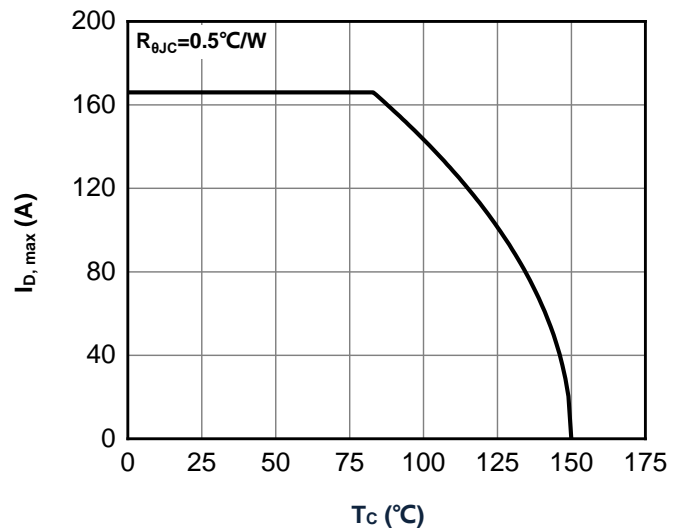
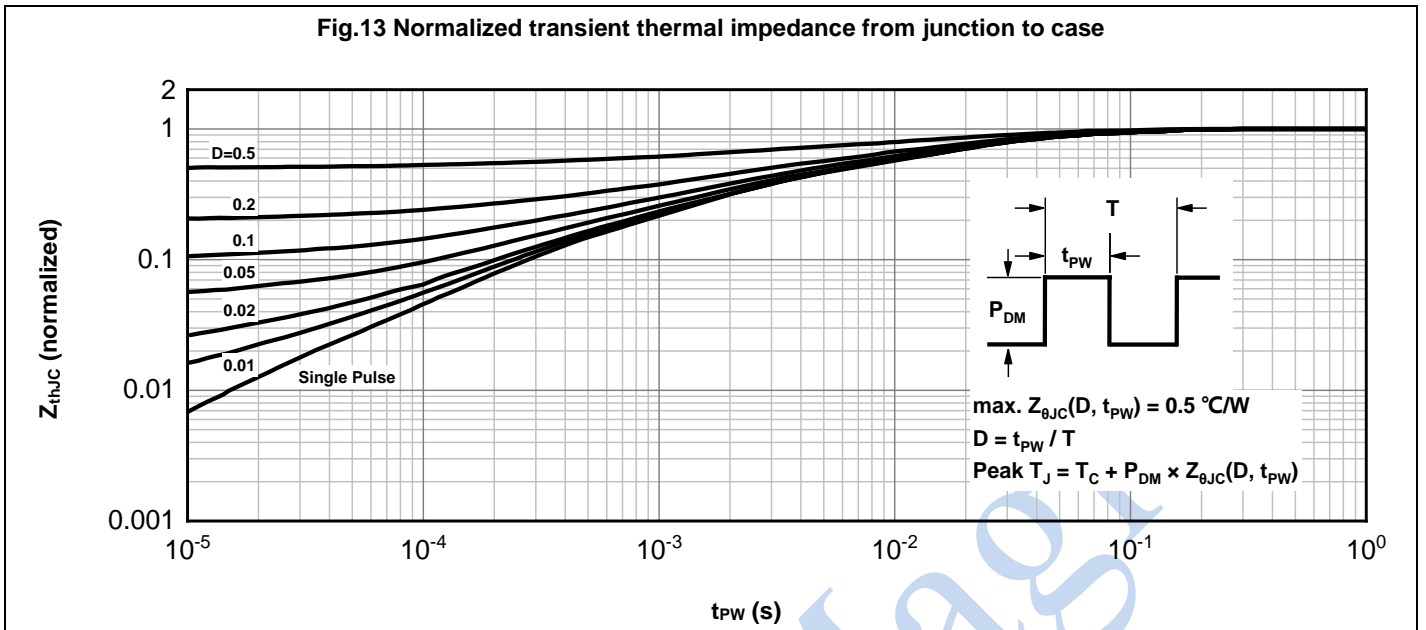
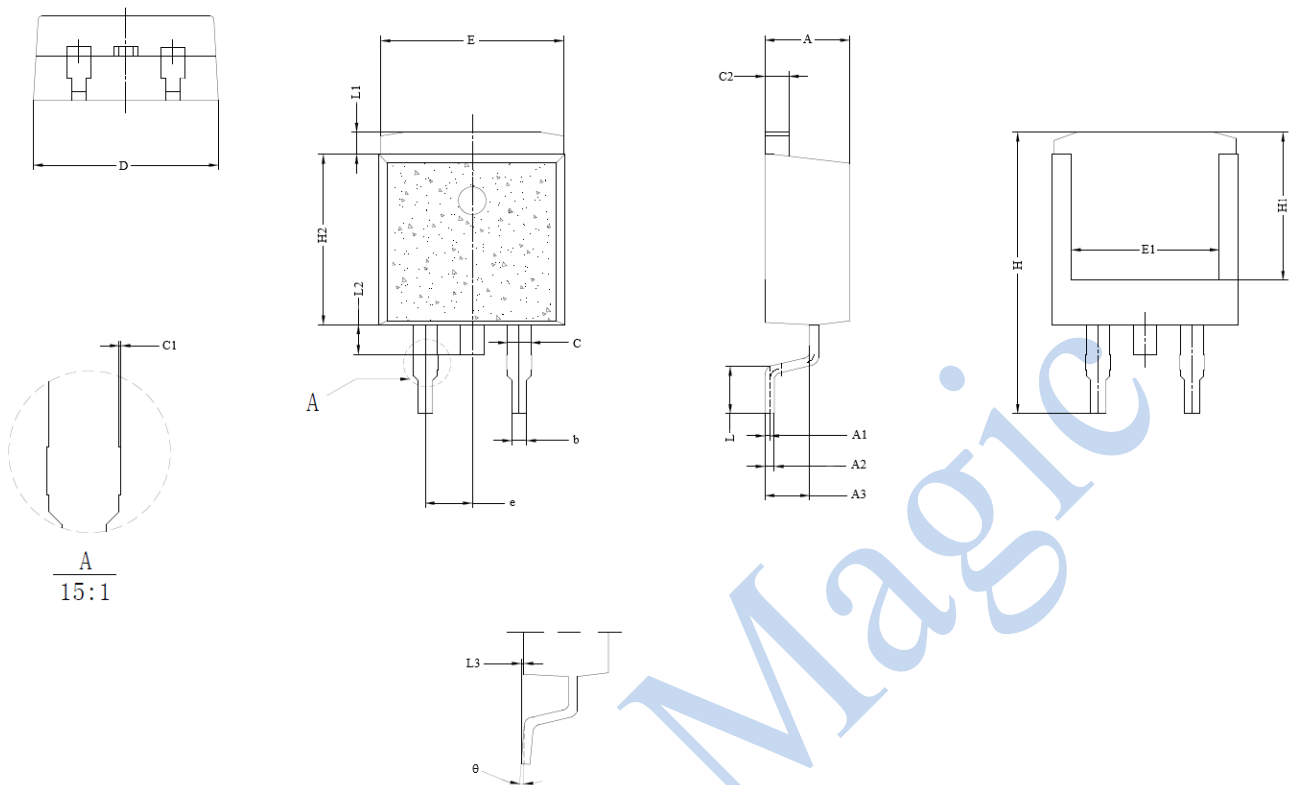


Fig.13 Normalized transient thermal impedance from junction to case



Silicon Magic

5. Package outline dimensions


Dim	Millimeters		
	Min	Nom	Max
A	4.47	4.57	4.67
A1	-	0.25	-
A2	-	0.50	-
A3	2.34	2.40	2.46
b	0.70	0.80	0.90
C	1.20	1.27	1.35
C1	-	-	0.08
C2	-	1.30	-
D	9.90	10.00	10.10
E	9.73	9.88	10.03
E1	7.50	8.00	8.50
e	2.54 BSC		
H	15.00	15.40	15.80
H1	7.50	8.00	8.15
H2	9.00	9.20	9.40
L	1.70	2.00	2.30
L1	1.05	1.25	1.45
L2	1.40	1.60	1.78
L3	0.00	-	0.25
θ	0°	-	5°

Legal Disclaimer

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Silicon Magic Technologies reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Silicon Magic Technologies or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Silicon Magic Technologies in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Silicon Magic Technologies or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory.