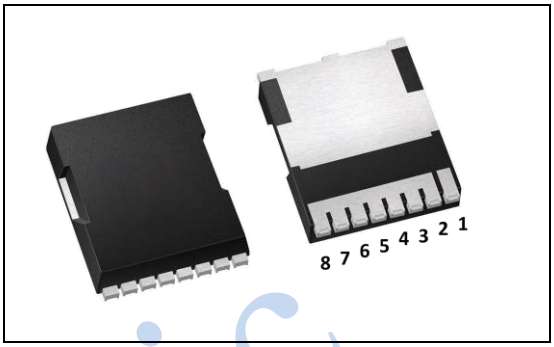
N-Channel 100 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
100	1.5 @ V_{GS} = 10V	330 (1)

TOLL

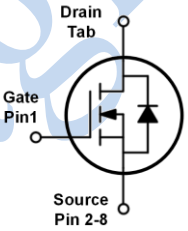


Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- Motor drives



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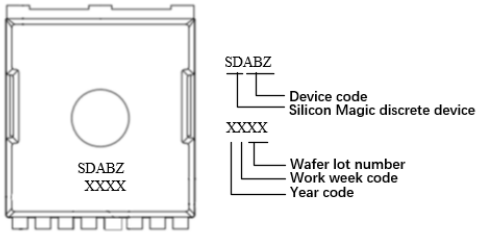


Package and ordering information

Ordering code	Package	Device code
SDN10N1P5S2T-1	TOLL	ABZ

1. Maximum ratings

Absolute maximum ratings (T_A = 25℃ unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	T_C=25℃ (1)	I_D	330	A
	T_C=100℃		285	
	T_A=25℃ (4)		34	
Pulsed drain current(2)		$I_{D,pulse}$	1320	
Avalanche energy, single pulse(3)		E_{AS}	1750	mJ
Power dissipation	T_C=25℃	P_D	517	W
	T_A=25℃ (4)		3.7	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 175	℃

2. Thermal resistance ratings

Thermal resistance ratings				
Parameter		**Symbol**	**Max.**	**Unit**
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.29	℃/W
Thermal resistance, junction-to-ambient (4)	Steady state	$R_{\theta JA}$	40	

3. Electrical characteristics

Electrical characteristics						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	100			V
Gate-source threshold voltage(6)	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2.45		2.95	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 100 A		1.1	1.5	mΩ
Forward transconductance(5)	g_{fs}	V_{DS} = 5 V, I_D = 100 A		280		S
Gate resistance	R_g	f = 1 MHz, open drain		1	2	Ω
Dynamic(5)						
Total gate charge	Q_g	V_{DS} = 50 V, I_D = 100 A, V_{GS} = 10 V		258	362	nC
Gate-source charge	Q_{gs}			68	96	
Gate-drain charge	Q_{gd}			74	104	
Turn-on delay time	$t_{d(on)}$	V_{DS} = 50 V, I_D = 100 A, V_{GS} = 10 V, R_{GEN} = 6 Ω		64	128	ns
Rise time	t_r			61	122	
Turn-off delay time	$t_{d(off)}$			221	442	
Fall time	t_f			104	208	
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		15650	21910	pF
Output capacitance	C_{oss}			2100	2940	
Reverse transfer capacitance	C_{rss}			45	90	
Reverse Diode Characteristics(5)						
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 100 A		0.8	1.1	V
Reverse recovery time	t_{rr}	V_{DS} = 50 V,I_F = 100 A, di/dt = 100 A/μs		126	227	ns
Reverse recovery charge	Q_{rr}			427	769	nC

Notes

(1) Package limited.

(2) Pulse width limited by maximum junction temperature.

(3) V_{DS} = 75 V, V_{GS} = 10 V, L = 0.3 mH.

(4) $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.

(5) Guaranteed by design, not subject to production testing.

(6) $V_{GS(th)}$ is in two grades:2.45V ≤ $V_{GS(th)}$ ≤ 2.70V and 2.70V < $V_{GS(th)}$ ≤ 2.95V.

4. Electrical characteristics diagrams

Fig.1 Typ. transfer characteristics

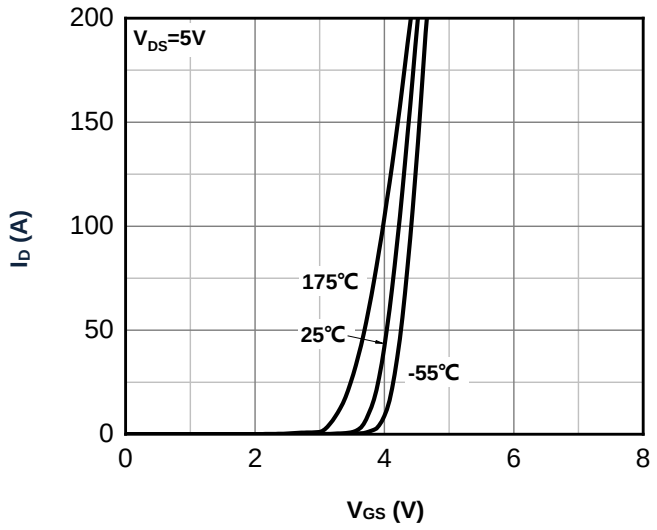


Fig.2 Typ. output characteristics

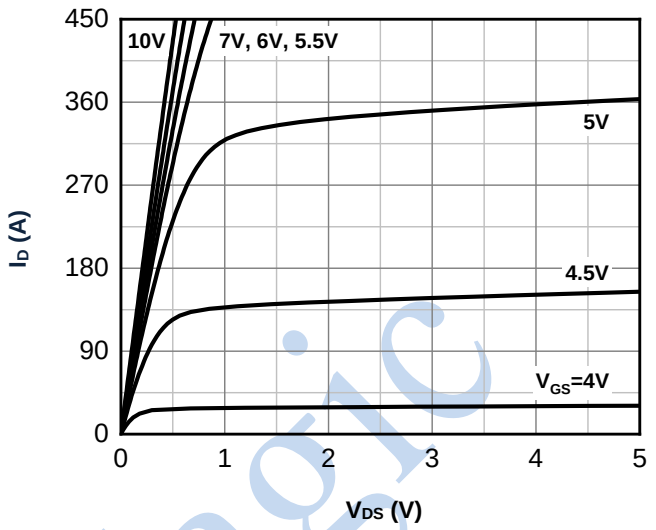


Fig.3 Normalized on-resistance vs drain current

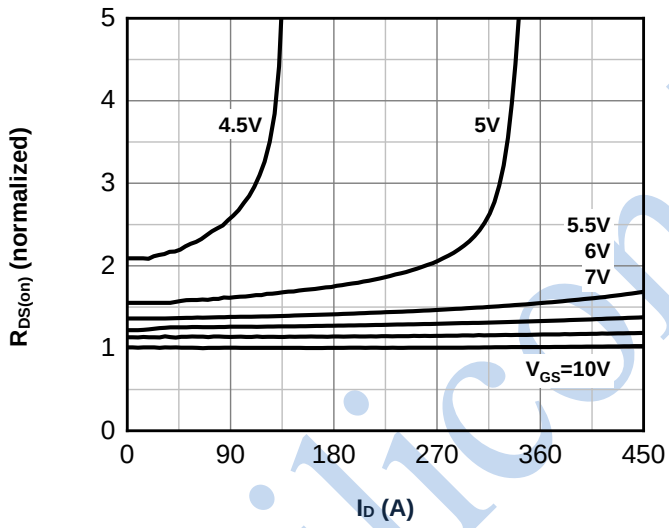


Fig.4 Typ. on-resistance vs gate-source voltage

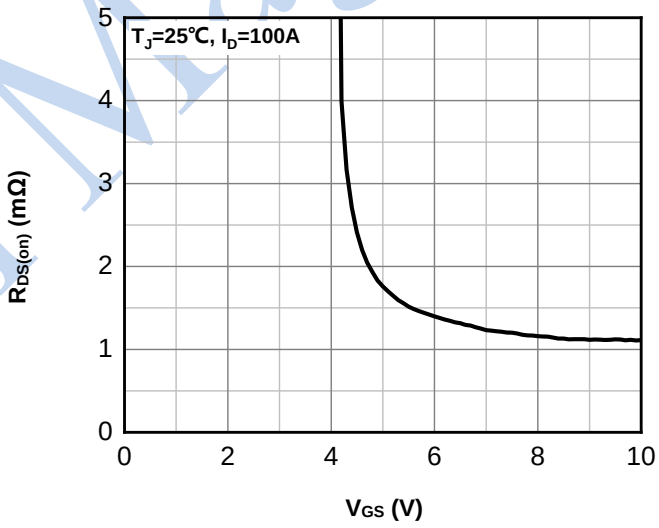


Fig.5 Normalized on-resistance vs junction temperature

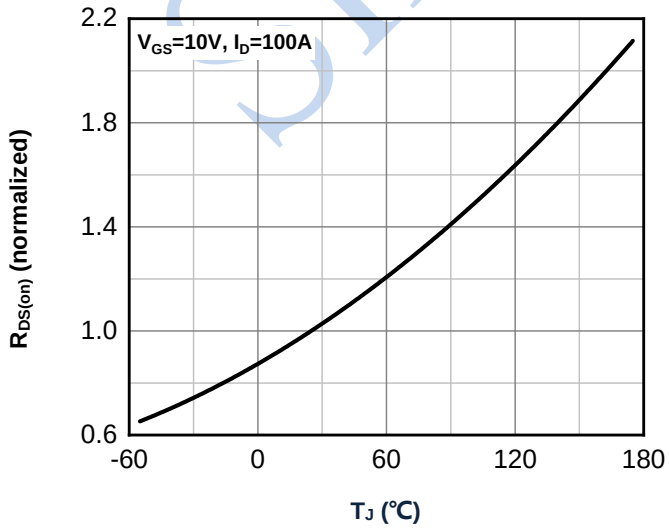


Fig.6 Typ. gate charge

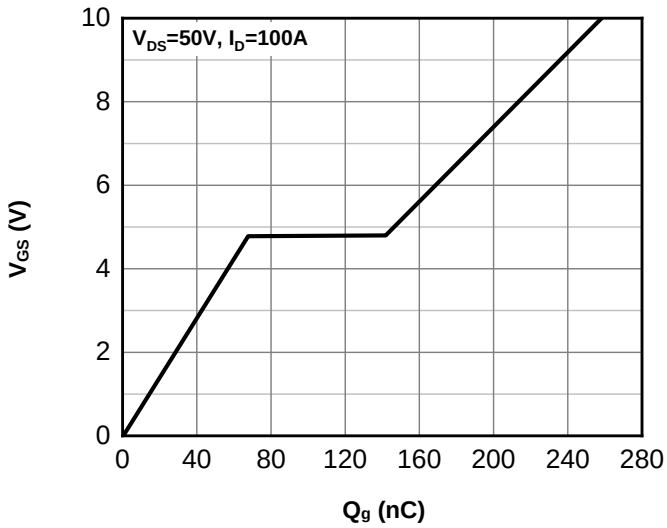


Fig.7 Typ. forward characteristics of body diode

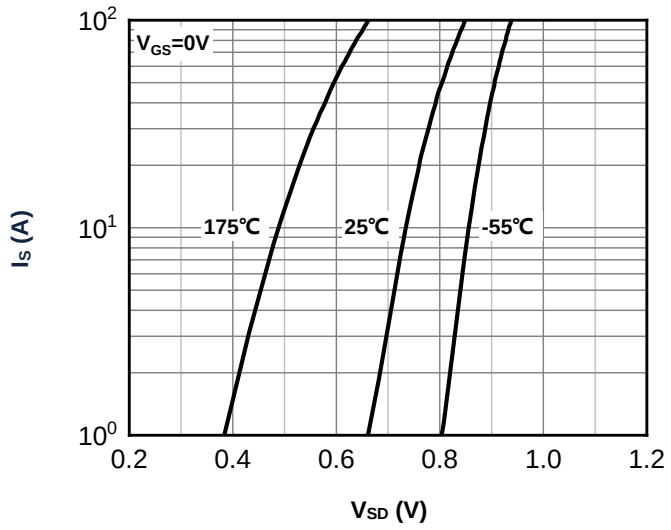


Fig.8 Safe operating area

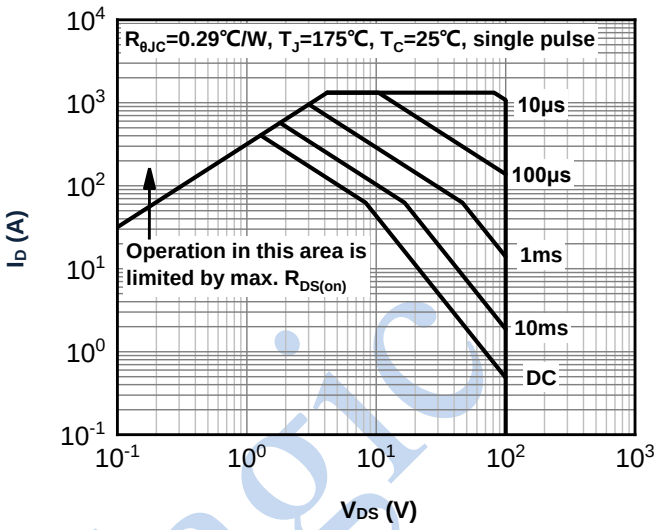


Fig.9 Typ. Capacitance

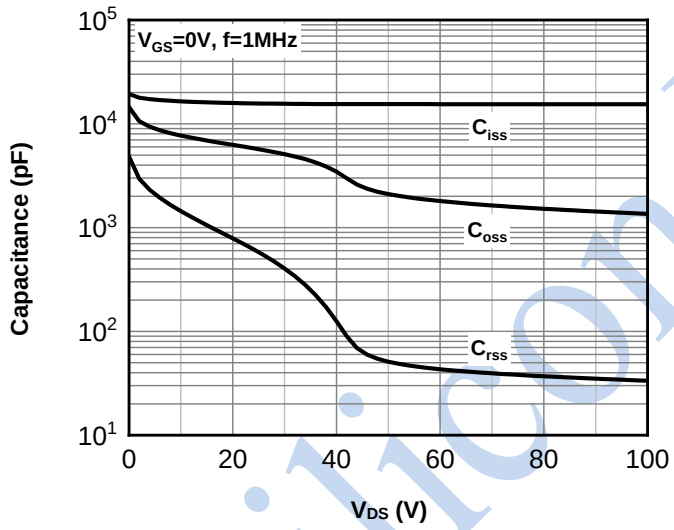


Fig.10 Single pulse maximum power dissipation

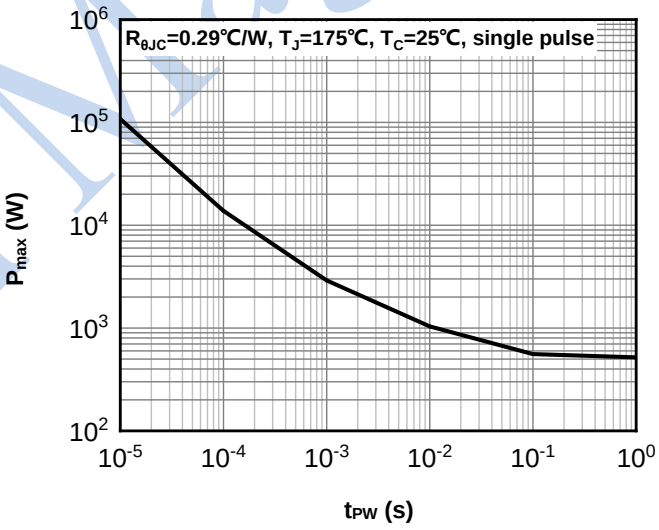


Fig.11 Max. power dissipation vs case temperature

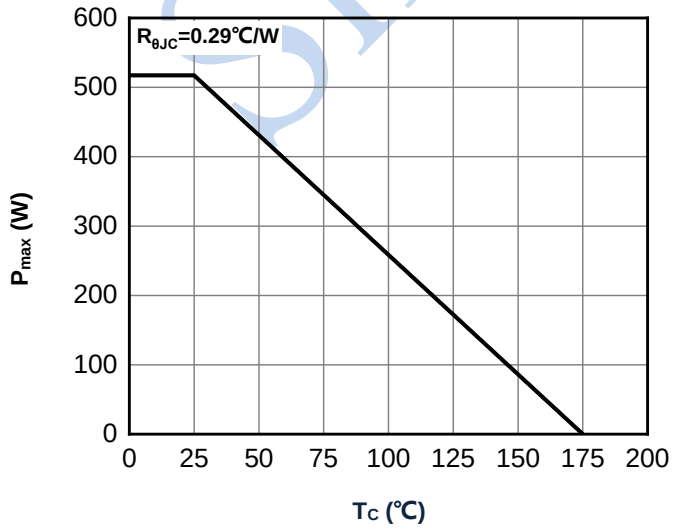


Fig.12 Max. continuous drain current vs case temperature

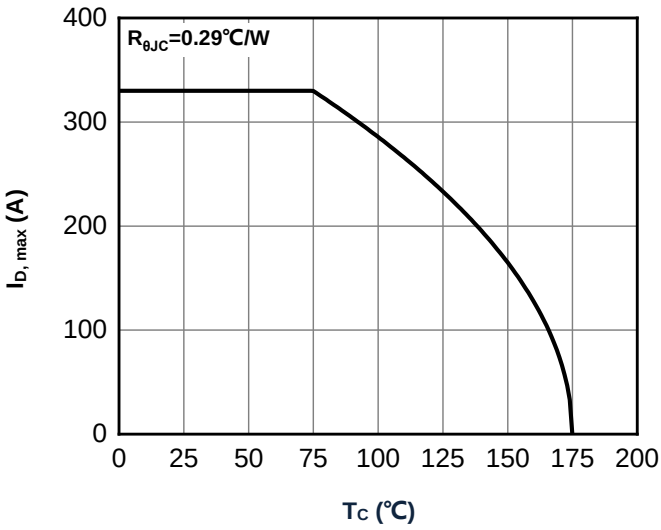


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

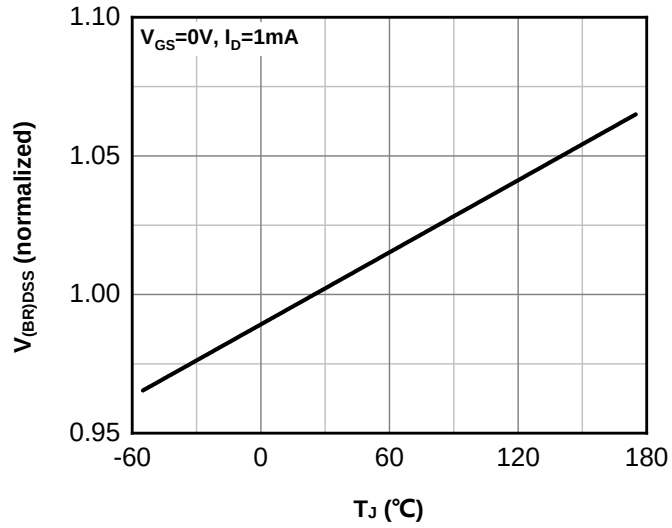


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

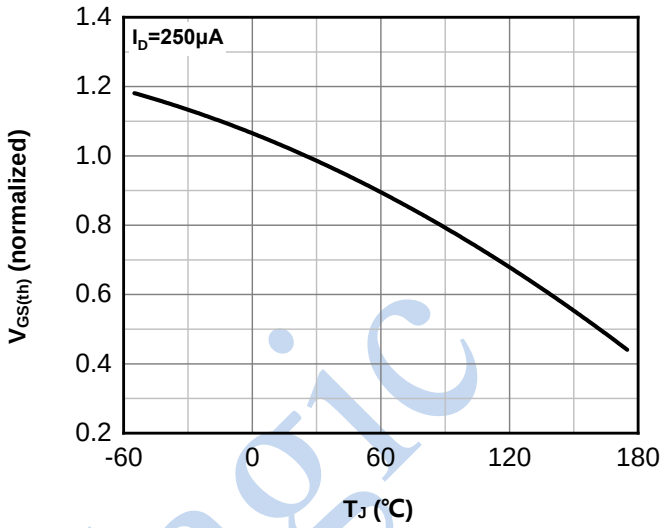
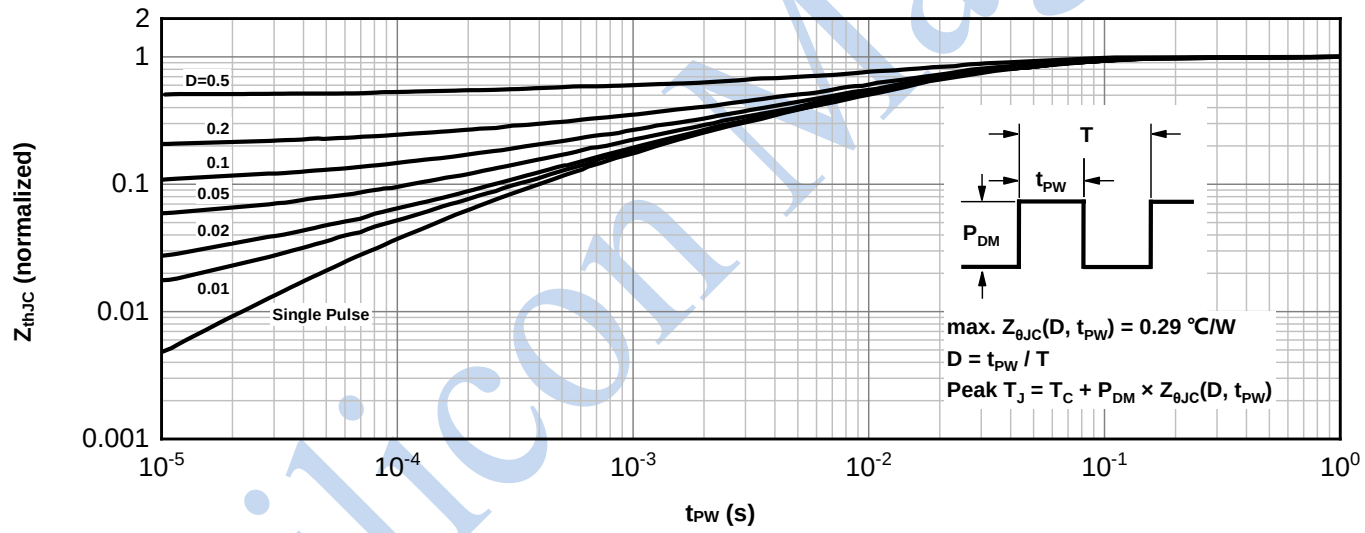
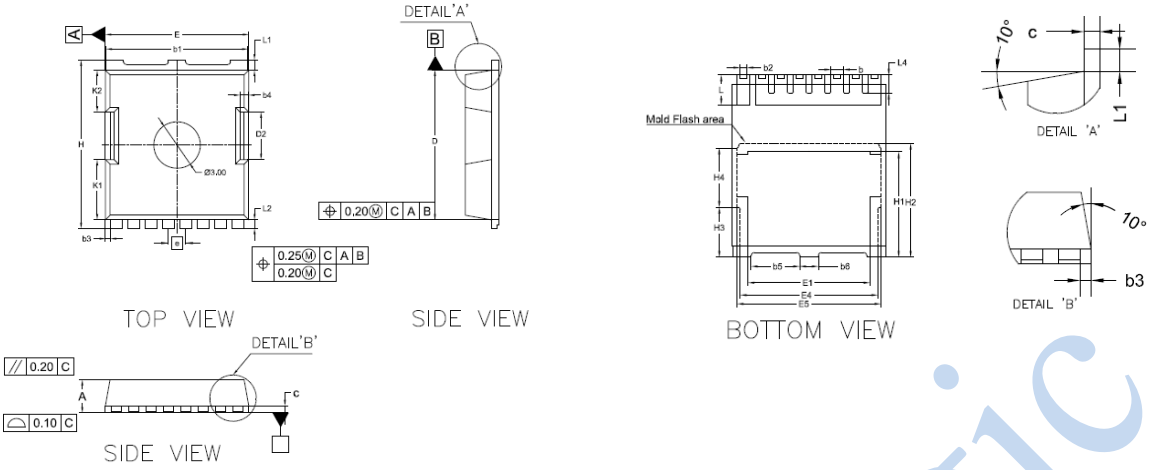


Fig.15 Normalized transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	2.200	2.300	2.400
c	0.492	0.500	0.508
D	10.280	10.380	10.480
E	9.800	9.900	10.000
e		1.20 BSC	
H	11.580	11.680	11.780
H1	6.650	6.750	6.850
H2		7.300	
H3		3.200	
H4		3.800	
K1		4.180	
K2		2.900	
D2		3.300	
b	0.700	0.800	0.900
b1	9.700	9.800	9.900
b2	0.420	0.460	0.500
b3		0.350	
b4		0.600	
b5		3.100	
b6		1.200	
L	1.700	1.900	2.100
L1		0.700	
L2		0.600	
L4	1.050	1.150	1.250
L5	0.500	0.600	0.700
E1		7.800	
E4		8.800	
E5		9.200	

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