

N-Channel 100 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
100	1.5 @ $V_{GS} = 10V$	330 ⁽¹⁾

Features

- Low $R_{DS(on)}$ trench technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

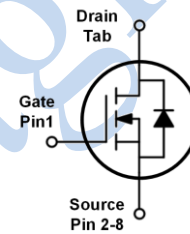
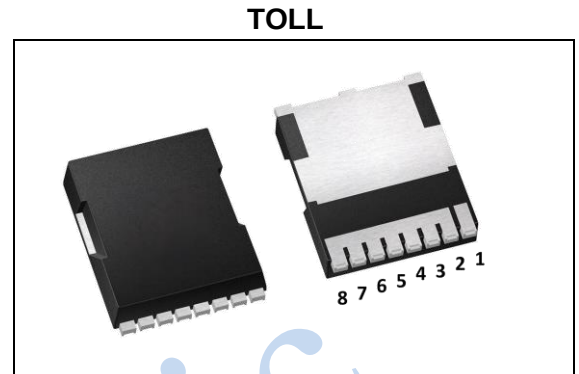
Applications

- DC/DC conversion
- Power switch
- Motor drives

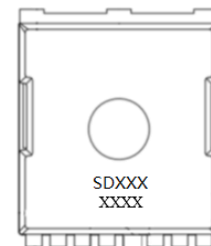
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Package and ordering information

Ordering code	Package	Device code
SDH10N1P5T-AB	TOLL	AGH



RoHS
COMPLIANT
HALOGEN
FREE



SDXXX
Device code
Silicon Magic discrete device

XXXX
Wafer lot number
Work week code
Year code

1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	$T_C = 25^\circ\text{C}$ ⁽¹⁾	I_D	330	A
	$T_C = 100^\circ\text{C}$		285	
	$T_A = 25^\circ\text{C}$ ⁽⁴⁾		34	
Pulsed drain current ⁽²⁾		$I_{D,pulse}$	1320	
Avalanche energy, single pulse ⁽³⁾		E_{AS}	1750	mJ
Power dissipation	$T_C = 25^\circ\text{C}$	P_D	517	W
	$T_A = 25^\circ\text{C}$ ⁽⁴⁾		3.7	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

2. Thermal resistance ratings

Thermal resistance ratings						
Parameter		Symbol	Max.	Unit		
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.29	°C/W		
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	40			

3. Electrical characteristics

Electrical characteristics						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	100			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.2	3	3.8	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 100\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 100\text{ A}$		1.1	1.5	m Ω
Forward transconductance ⁽⁵⁾	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 100\text{ A}$		280		S
Gate resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		1	2	Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q_g	$V_{DS} = 50\text{ V}, I_D = 100\text{ A}, V_{GS} = 10\text{ V}$		258	362	nC
Gate-source charge	Q_{gs}			68	96	
Gate-drain charge	Q_{gd}			74	104	
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 50\text{ V}, I_D = 100\text{ A}, V_{GS} = 10\text{ V},$ $R_{GEN} = 6\text{ }\Omega$		64	128	ns
Rise time	t_r			61	122	
Turn-off delay time	$t_{d(off)}$			221	442	
Fall time	t_f			104	208	
Input capacitance	C_{iss}	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		15650	21910	pF
Output capacitance	C_{oss}			2100	2940	
Reverse transfer capacitance	C_{rss}			45	90	
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_F = 100\text{ A}$		0.8	1.1	V
Reverse recovery time	t_{rr}	$V_{DS} = 50\text{ V}, I_F = 100\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		126	227	ns
Reverse recovery charge	Q_{rr}			427	769	nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 75\text{ V}, V_{GS} = 10\text{ V}, L = 0.3\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

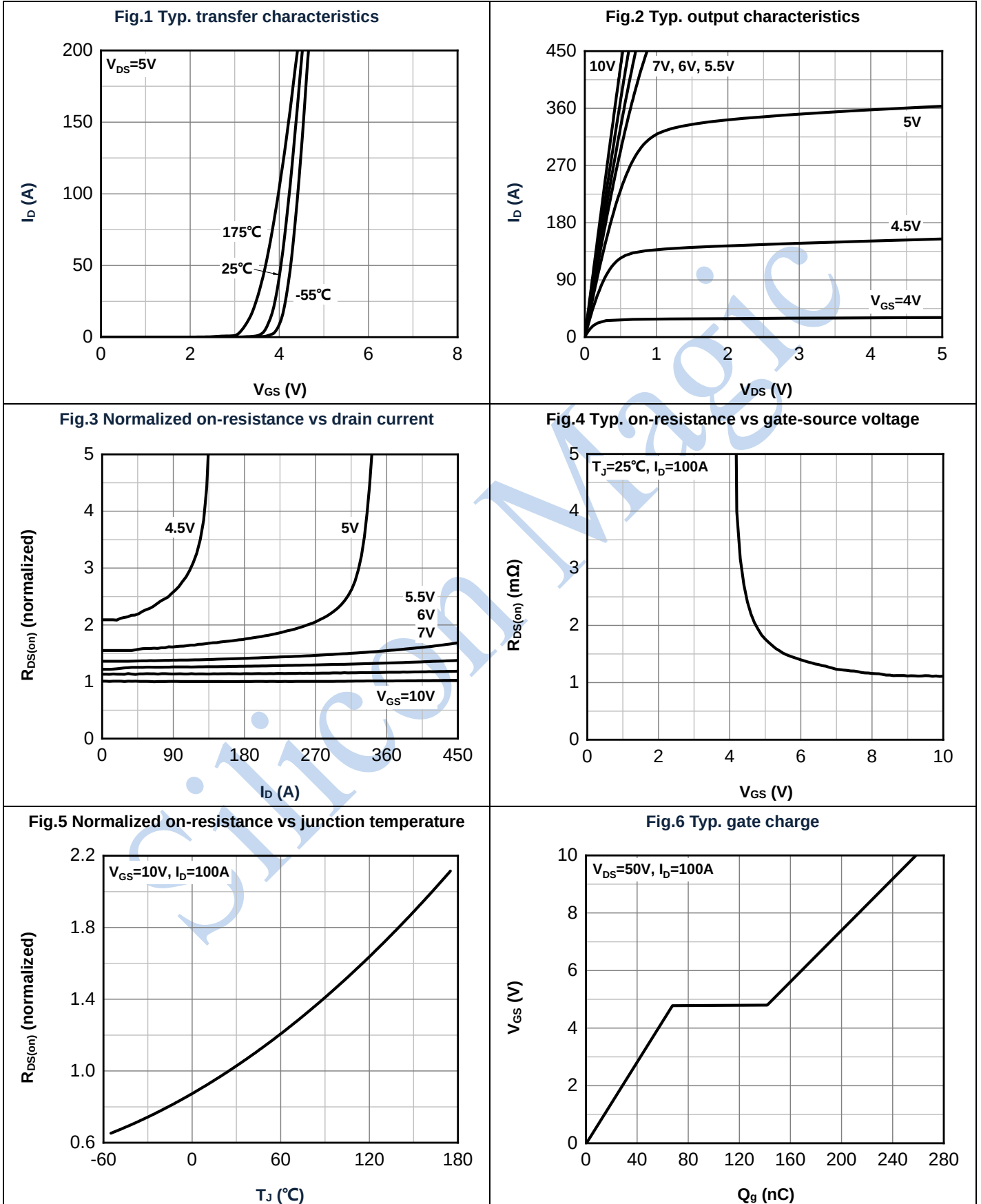


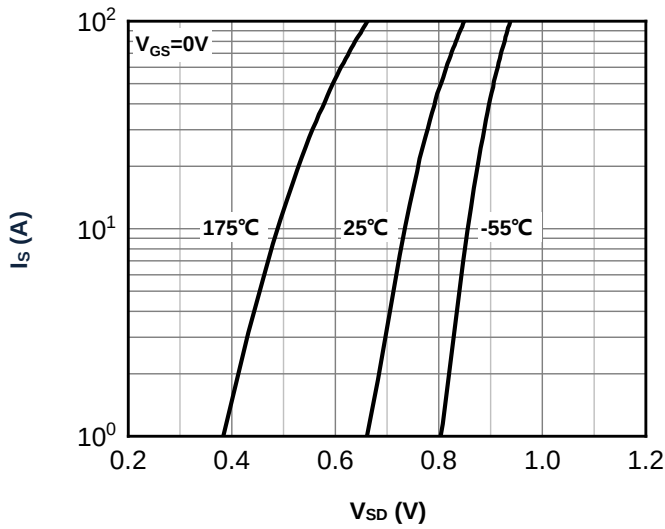
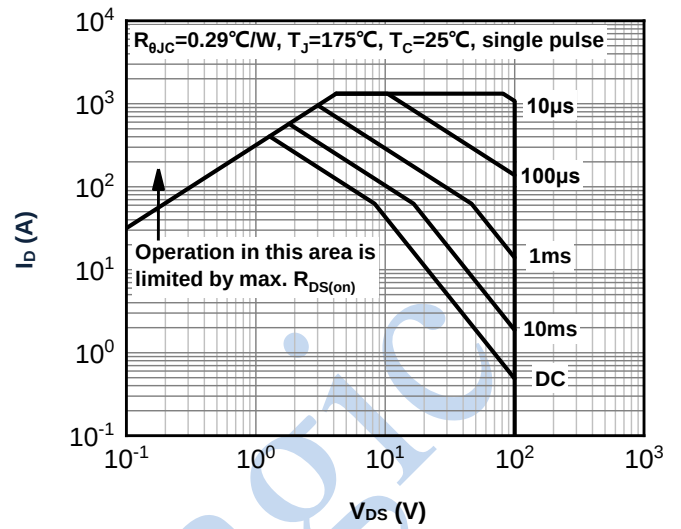
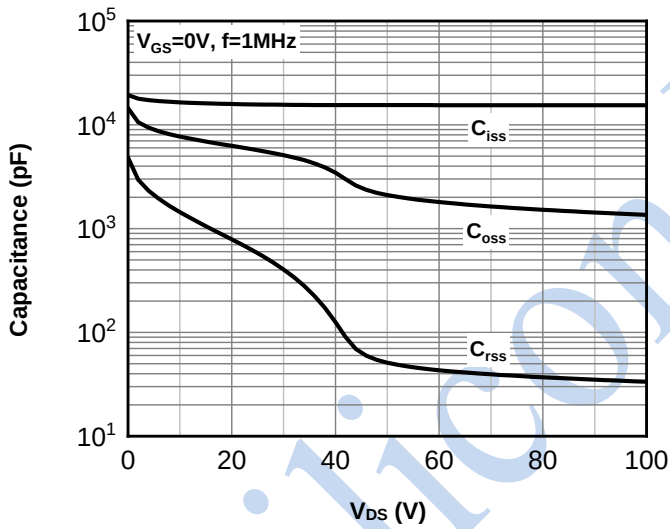
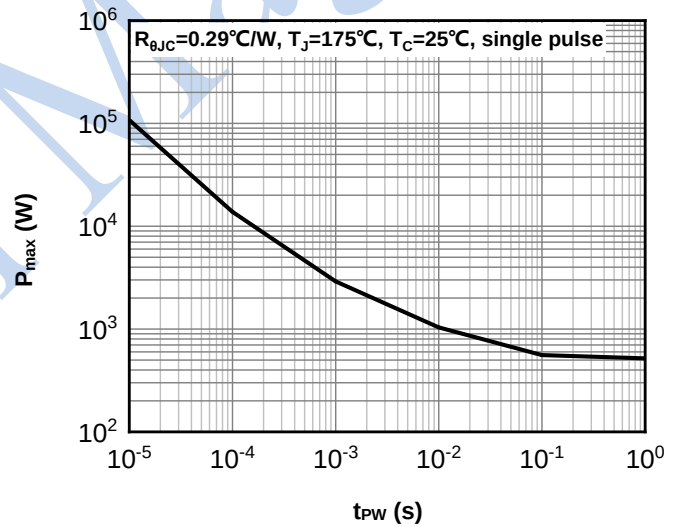
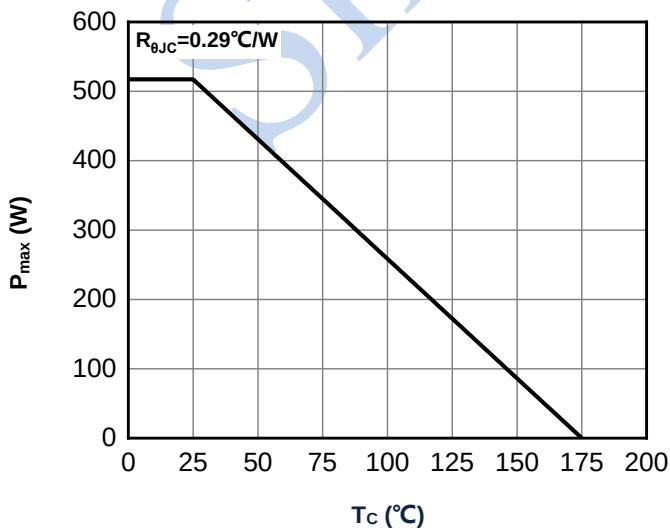
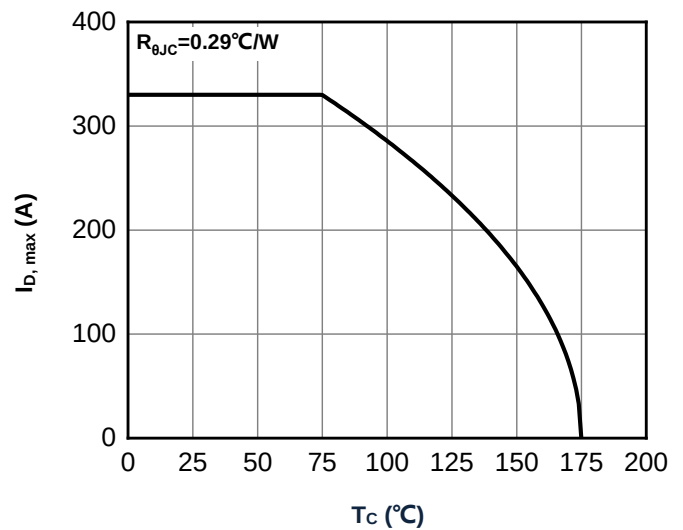
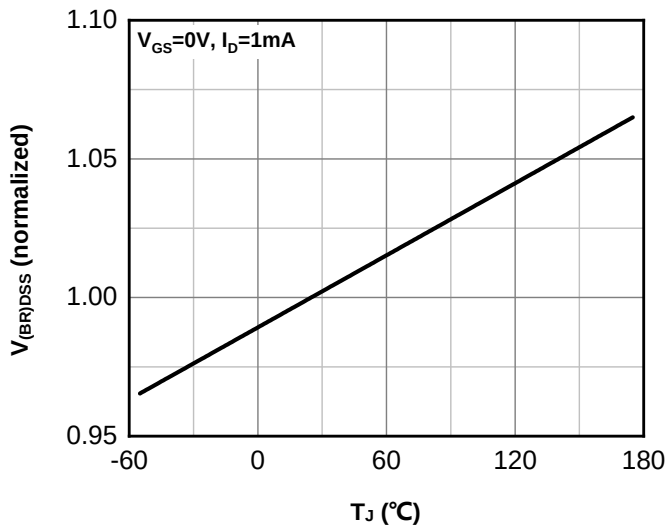
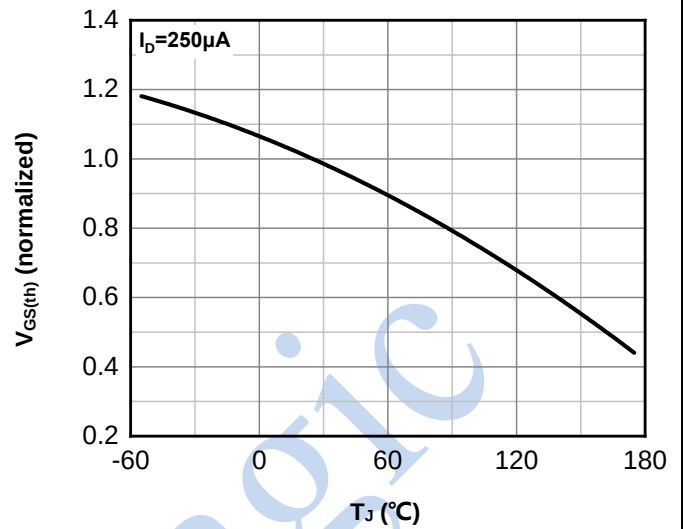
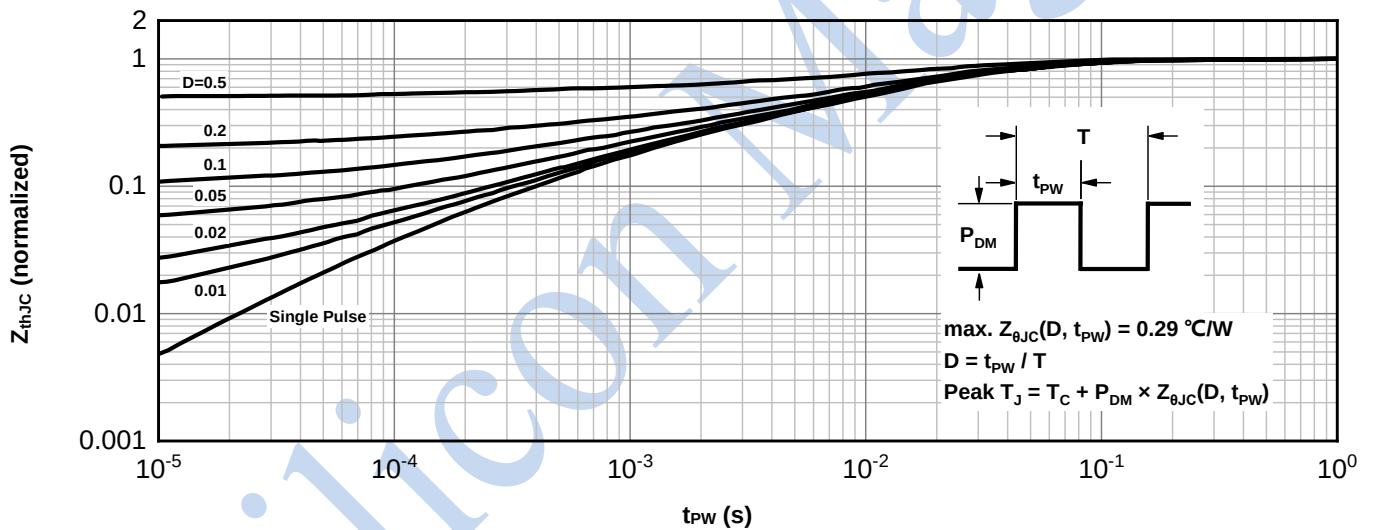
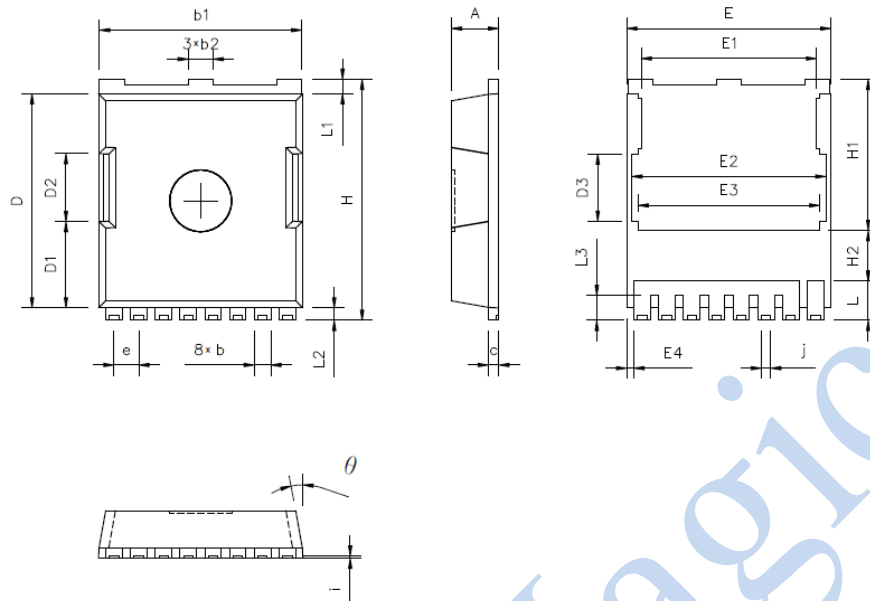
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

Fig.15 Normalized transient thermal impedance from junction to case


5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	2.20	-	2.40
b	0.70	-	0.90
b1	9.70	-	9.90
b2	1.20 REF		
c	0.40	-	0.60
D	10.28	-	10.48
D1	4.08	-	4.28
D2	3.20	-	3.40
D3	3.16	-	3.36
E	9.80	-	10.00
E1	8.40	-	8.60
E2	9.30	-	9.50
E3	8.80 REF		
E4	0.25	-	0.45
e	1.20 BASIC		
H	11.58	-	11.78
H1	7.23	-	7.43
H2	2.45 REF		
i	0.10	-	-
j	0.45 REF		
L	1.60	-	2.10
L1	0.60	-	0.80
L2	0.50	-	0.70
L3	1.05	-	1.30
θ	10° REF		

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