

Preliminary Specification: Subject to Change without Notice

N-Channel 60 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
60	3 @ $V_{GS} = 10V$	126 ⁽¹⁾

Features

- For automotive applications and AEC-Q101 compliant
- Great FOM (figure of merit) with low $R_{DS(on)}$ SGT technology
- Fast switching speed
- 100% avalanche tested. High avalanche ruggedness.

Applications

- DC/DC conversion
- Power switch
- Motor drives

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Package and ordering information

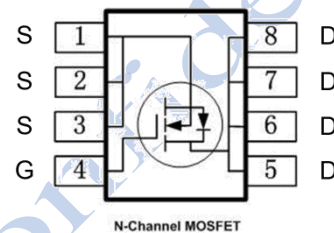
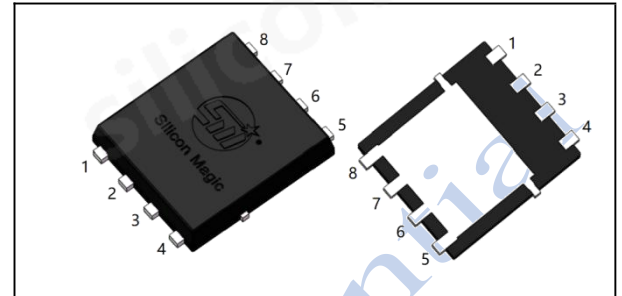
Ordering code	Package	Device code
SDA06N2P8CN-AA	PDFN5*6-8L	A06N2P8CN-AA

1. Maximum ratings

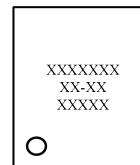
Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	60	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	$T_C = 25^\circ\text{C}$ ⁽¹⁾	126	A
	$T_C = 100^\circ\text{C}$	92	
	$T_A = 25^\circ\text{C}$ ⁽⁴⁾	23.2	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	504	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	247	mJ
Power dissipation	$T_C = 25^\circ\text{C}$	93.7	W
	$T_A = 25^\circ\text{C}$ ⁽⁴⁾	3	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

PDFN5*6-8L



RoHS
COMPLIANT
HALOGEN
FREE



XXXXXX
XX-XX
XXXXX

Device code

lot number
Work week code
Year code

2. Thermal resistance ratings

Thermal resistance ratings				
Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	1.6	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	50	

3. Electrical Characteristics

Electrical characteristics (T _J = 25°C unless otherwise noted)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	60			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.2	3.0	3.8	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±30 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 50 A		2.6	3	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 50 A		110		S
Gate resistance	R _g	f = 1 MHz		2.7		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 30 V, I _D = 50 A, V _{GS} = 10 V		39.1		nC
Gate-source charge	Q _{gs}			15.3		
Gate-drain charge	Q _{gd}			7.6		
Turn-on delay time	t _{d(on)}	V _{DS} = 30 V, I _D = 50 A, V _{GS} = 10 V, R _{GEN} = 1.6 Ω		15.6		ns
Rise time	t _r			11.4		
Turn-off delay time	t _{d(off)}			11.0		
Fall time	t _f			7.1		
Input capacitance	C _{iss}	V _{DS} = 30 V, V _{GS} = 0 V, f = 1 MHz		3038		pF
Output capacitance	C _{oss}			696		
Reverse transfer capacitance	C _{rss}			19		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 20 A		0.9	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 30 V, I _F = 50 A, di/dt = 100 A/μs		44		ns
Reverse recovery charge	Q _{rr}			45		nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, L = 0.1\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

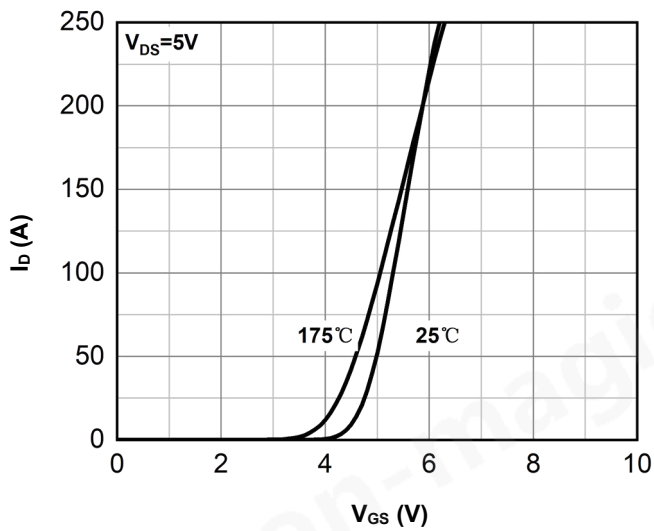
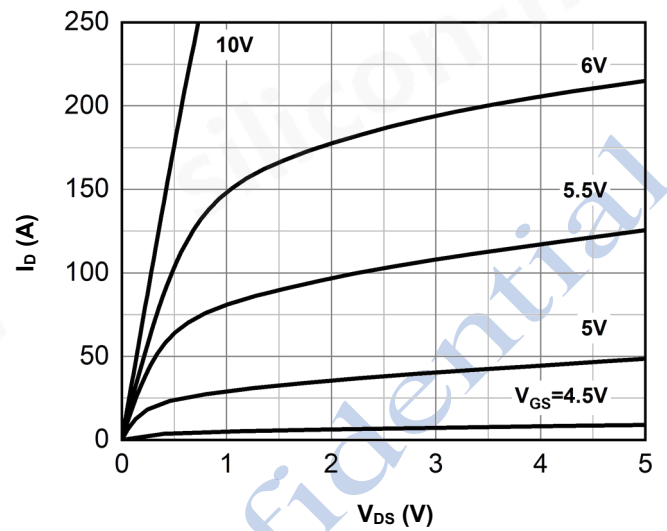
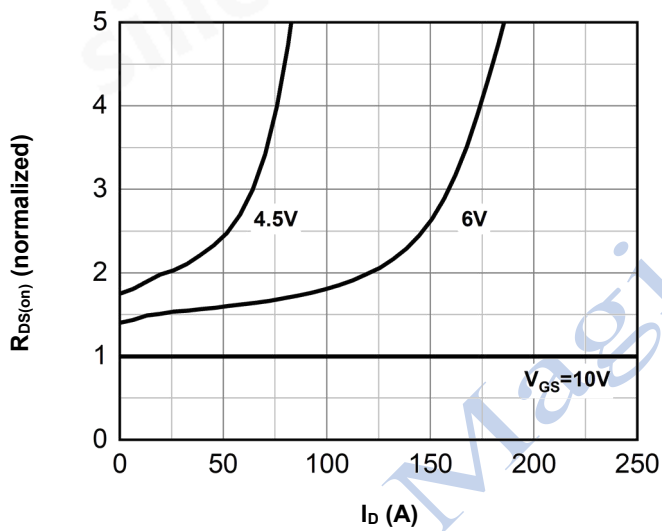
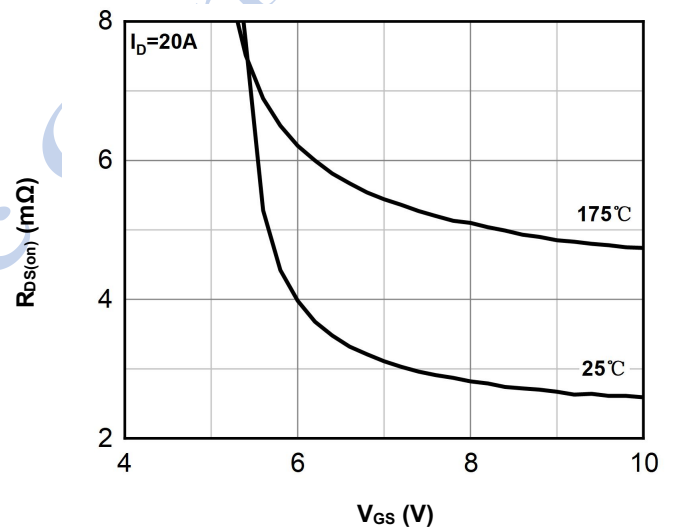
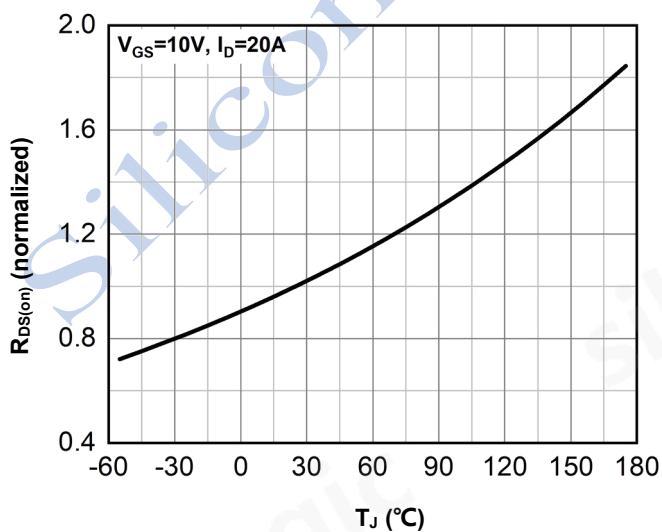
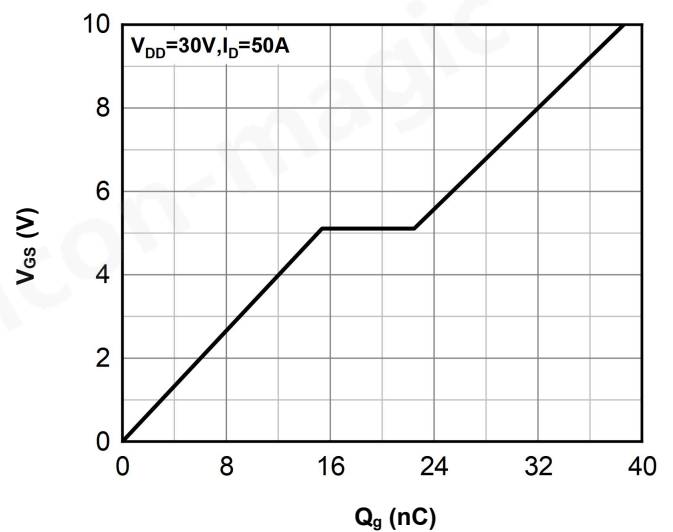
Fig.1 Typ. transfer characteristics

Fig.2 Typ. output characteristics

Fig.3 Normalized on-resistance vs drain current

Fig.4 Typ. on-resistance vs gate-source voltage

Fig.5 Normalized on-resistance vs junction temperature

Fig.6 Typ. gate charge


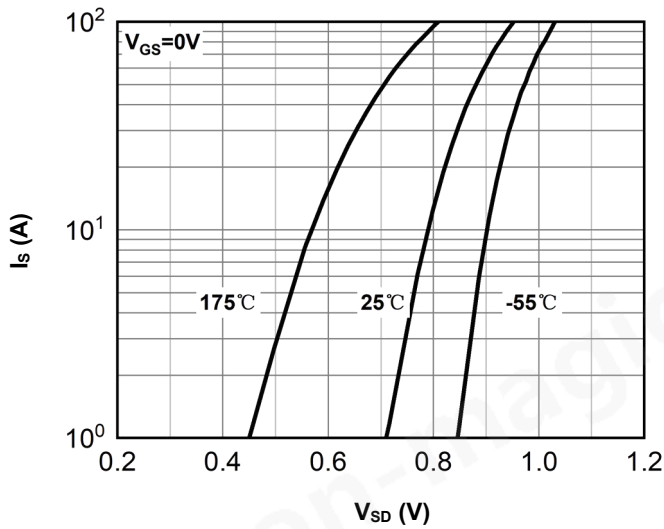
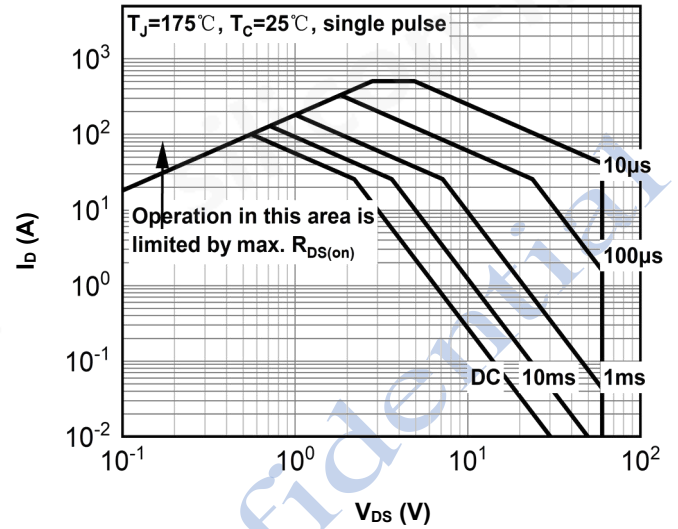
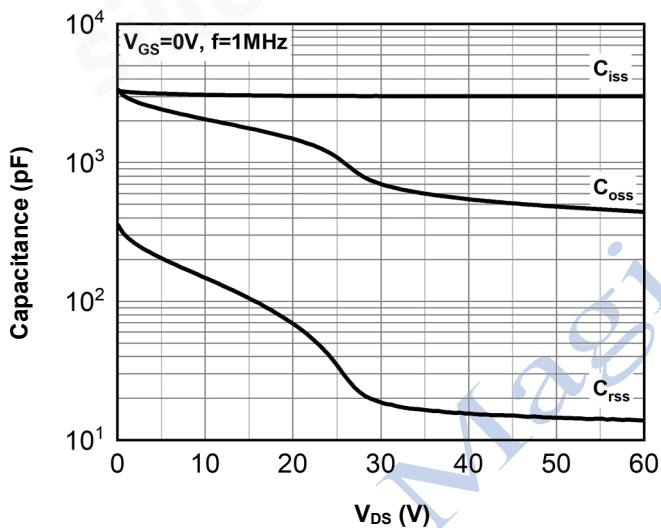
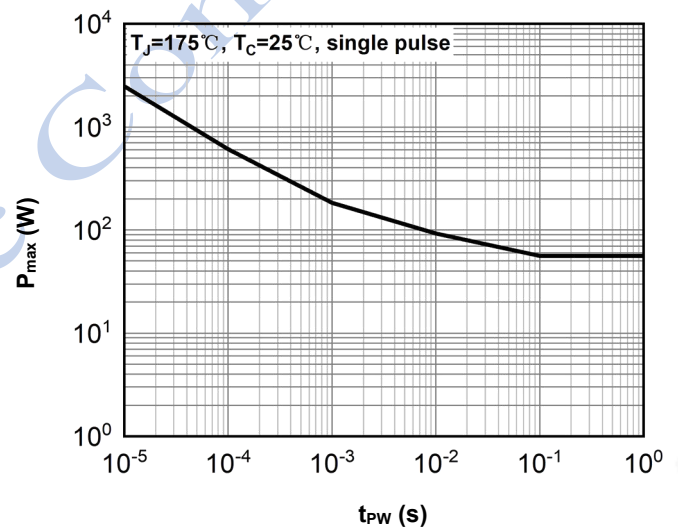
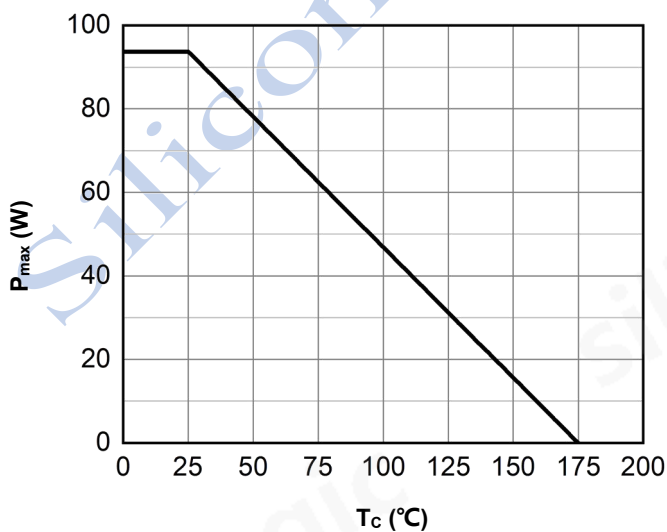
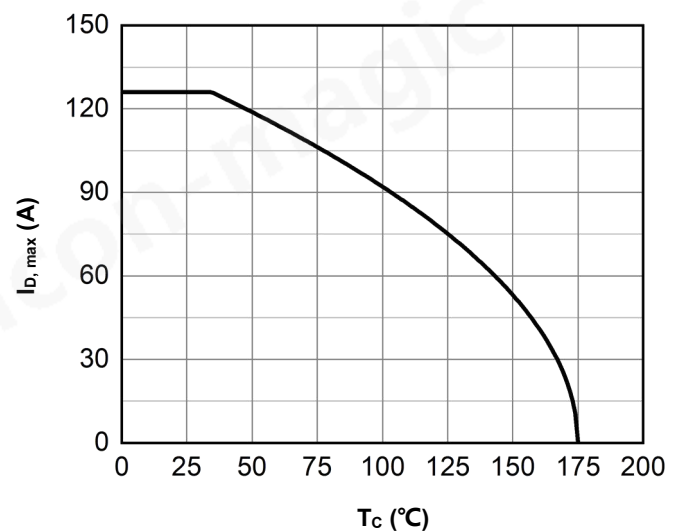
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

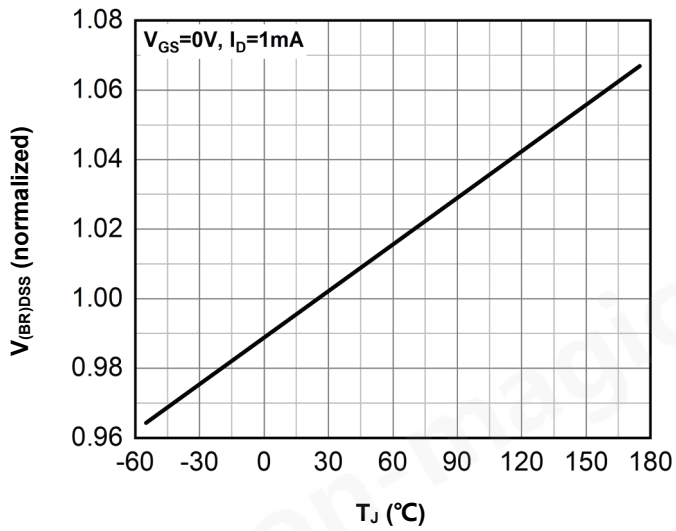


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

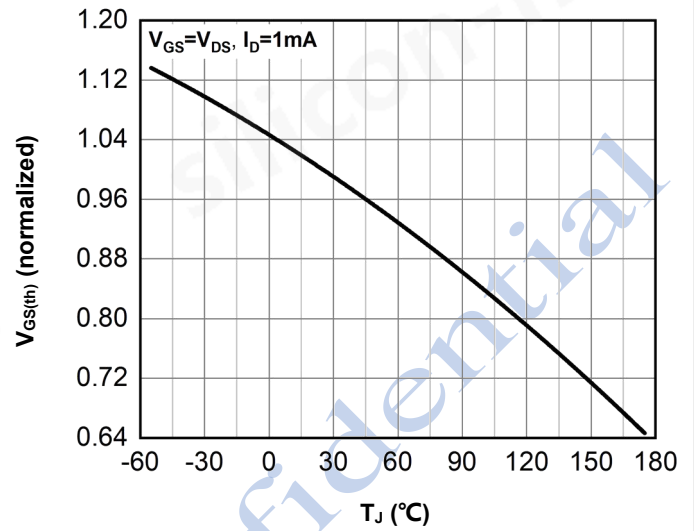
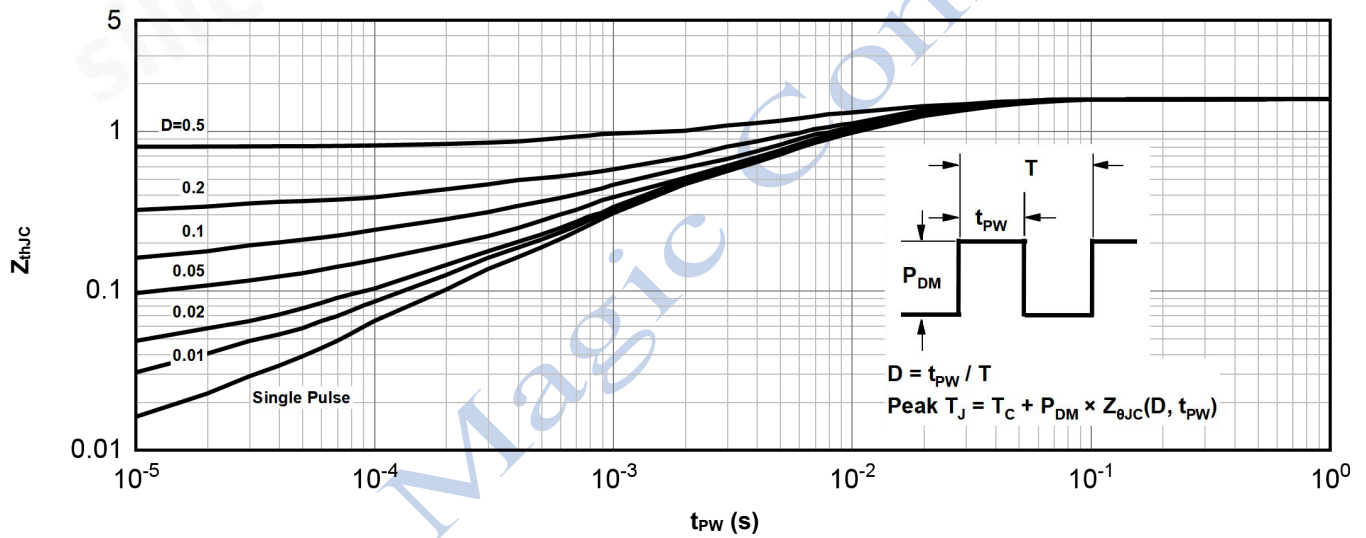
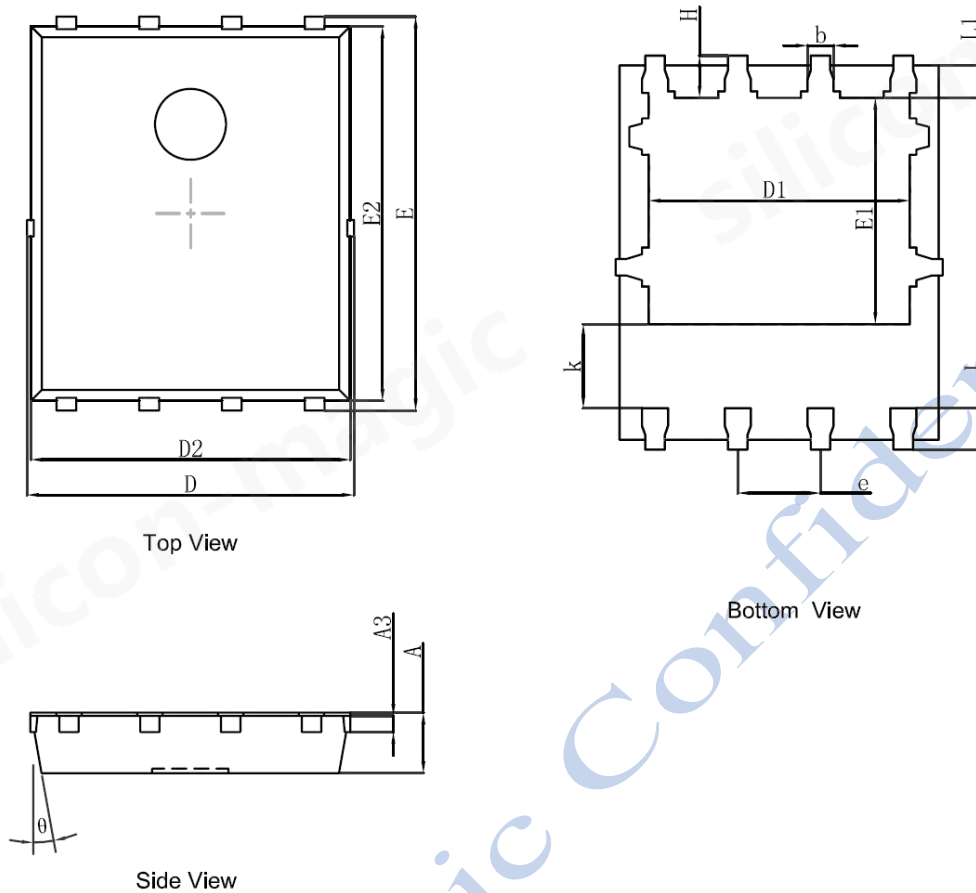


Fig.15 Transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	0.900	—	1.000
A3	0.254 REF		
D	4.944	—	5.096
E	5.974	—	6.126
D1	3.910	—	4.110
E1	3.375	—	3.575
D2	4.824	—	4.976
E2	5.674	—	5.826
k	1.190	—	1.390
b	0.350	—	0.450
e	1.270 TYP		
L	0.559	—	0.711
L1	0.424	—	0.576
H	0.574	—	0.726
θ	10°	—	12°

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