

Preliminary Specification: Subject to Change without Notice

N-Channel 40 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
40	1.0 @ $V_{GS} = 10V$	240 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- Motor drives

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Package and ordering information

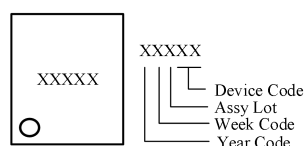
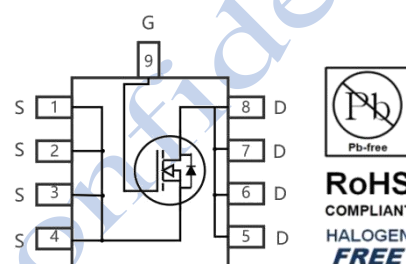
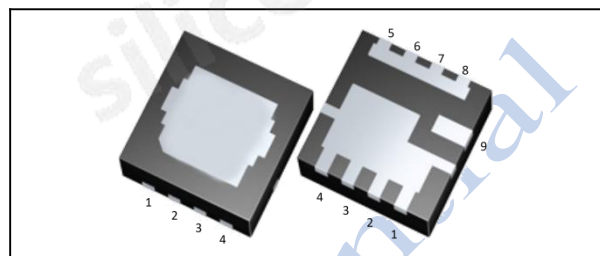
Ordering code	Package	Device code
SDH04L1P0ABN-BB	DFN3.3*3.3 Source Down DSC - Center Gate	TL

1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	40	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	$T_C=25^{\circ}\text{C}$ ⁽¹⁾	I_D	240	A
	$T_C=100^{\circ}\text{C}$		170	
	$T_A=25^{\circ}\text{C}$ ⁽⁴⁾		36	
Pulsed drain current ⁽²⁾		$I_{D,pulse}$	962	
Avalanche energy, single pulse ⁽³⁾		E_{AS}	210	mJ
Power dissipation	$T_C=25^{\circ}\text{C}$	P_D	107	W
	$T_A=25^{\circ}\text{C}$ ⁽⁴⁾		2.4	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 175	°C

DFN3.3*3.3 Source Down DSC Center Gate



2. Thermal resistance ratings

Thermal resistance ratings				
Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	1.4	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	62.5	

3. Electrical Characteristics

Electrical characteristics (T _J = 25°C unless otherwise noted)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	40			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	1.1	1.6	2.1	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 40 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		0.86	1.0	mΩ
		V _{GS} = 4.5 V, I _D = 10 A		1.44	1.8	
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 90 A		295		S
Gate resistance	R _g	f = 1 MHz		1.2		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 20 V, I _D = 45 A, V _{GS} = 4.5 V		25.7		nC
Total gate charge	Q _g	V _{DS} = 20 V, I _D = 90 A, V _{GS} = 10 V		51.9		nC
Gate-source charge	Q _{gs}			14.6		
Gate-drain charge	Q _{gd}			10.1		
Turn-on delay time	t _{d(on)}	V _{DS} = 20 V, I _D = 90 A, V _{GS} = 10 V, R _{GEN} = 1.6 Ω		10.9		ns
Rise time	t _r			10.7		
Turn-off delay time	t _{d(off)}			14.5		
Fall time	t _f			8.8		
Input capacitance	C _{iss}	V _{DS} = 20 V, V _{GS} = 0 V, f = 1 MHz		3697		pF
Output capacitance	C _{oss}			1313		
Reverse transfer capacitance	C _{rss}			44		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 90 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 20 V, I _F = 20 A, di/dt = 100 A/μs		32.6		ns
Reverse recovery charge	Q _{rr}			27.8		nC

Notes

- (1) Limited by maximum junction temperature.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, L = 1\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

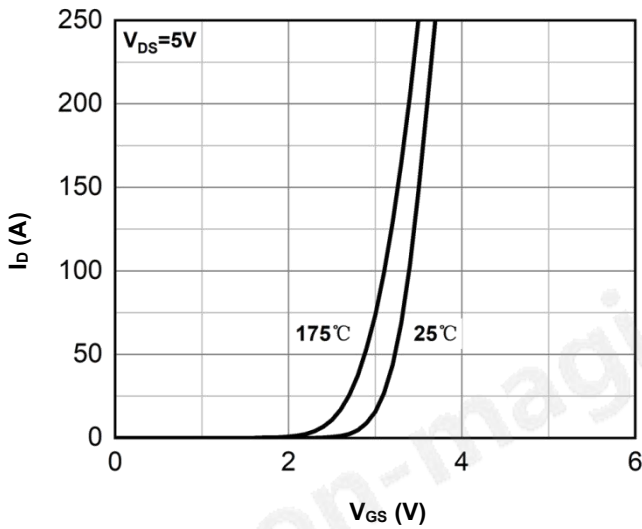
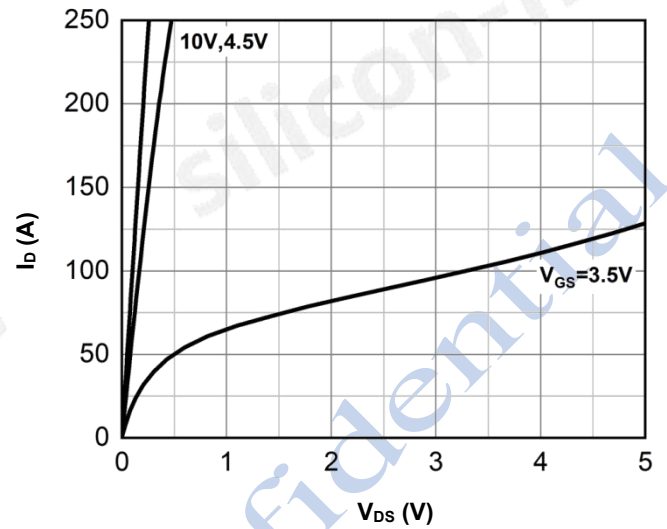
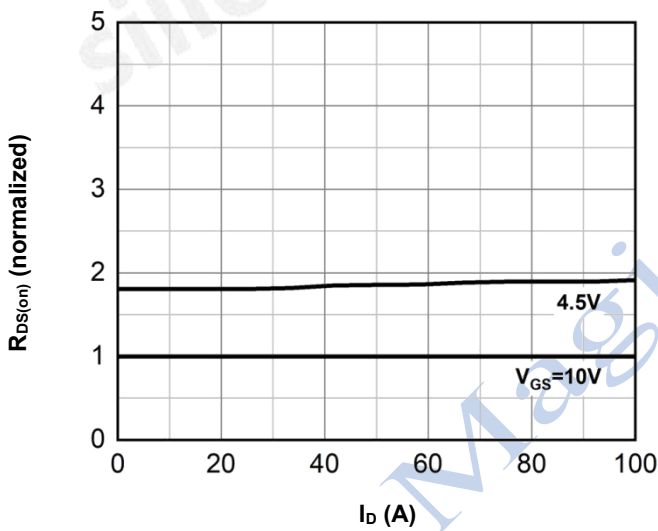
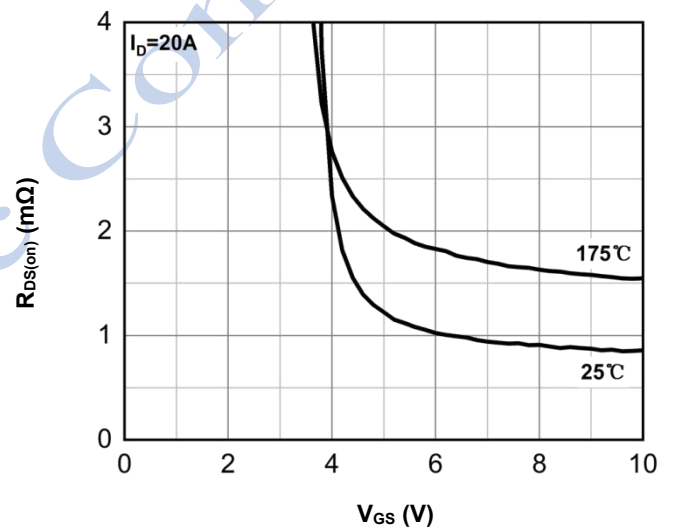
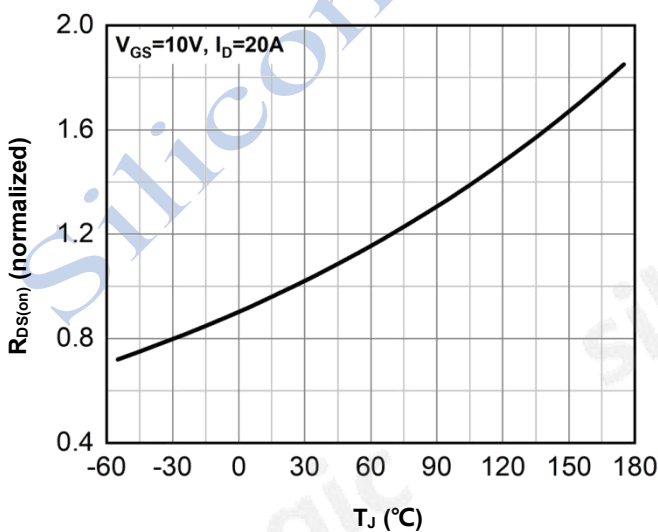
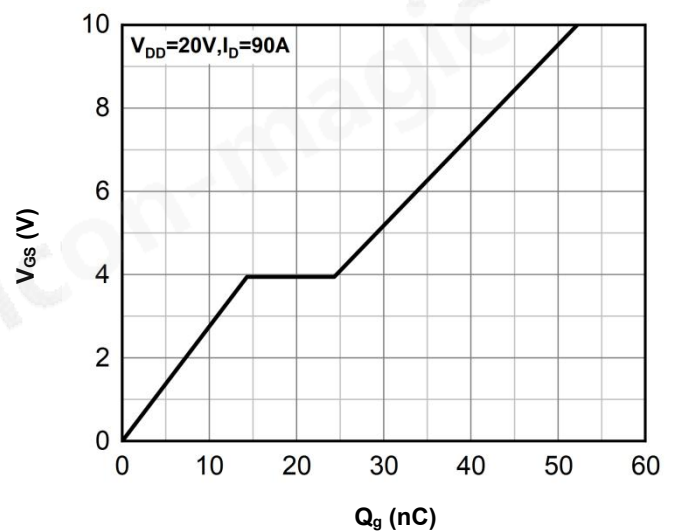
Fig.1 Typ. transfer characteristics

Fig.2 Typ. output characteristics

Fig.3 Normalized on-resistance vs drain current

Fig.4 Typ. on-resistance vs gate-source voltage

Fig.5 Normalized on-resistance vs junction temperature

Fig.6 Typ. gate charge


Fig.7 Typ. forward characteristics of body diode

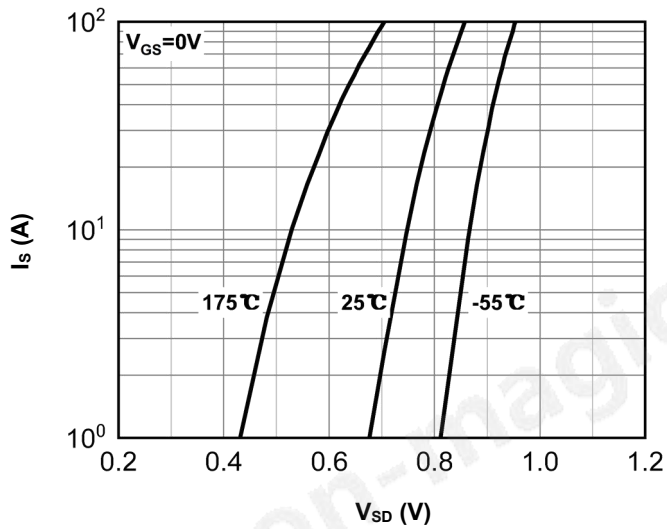


Fig.8 Safe operating area

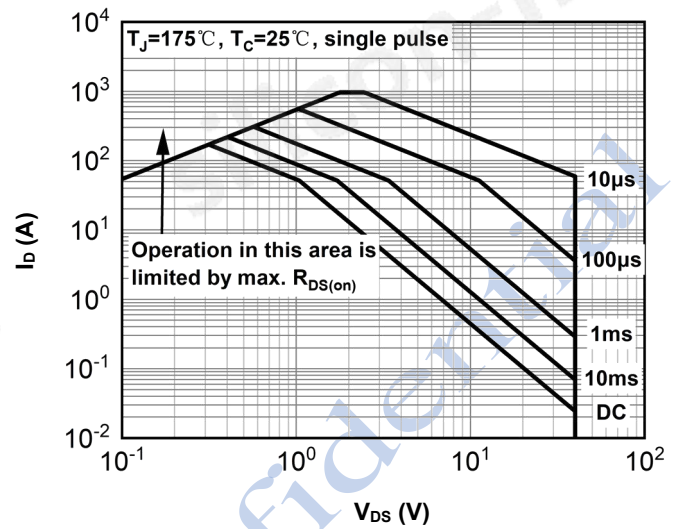


Fig.9 Typ. Capacitance

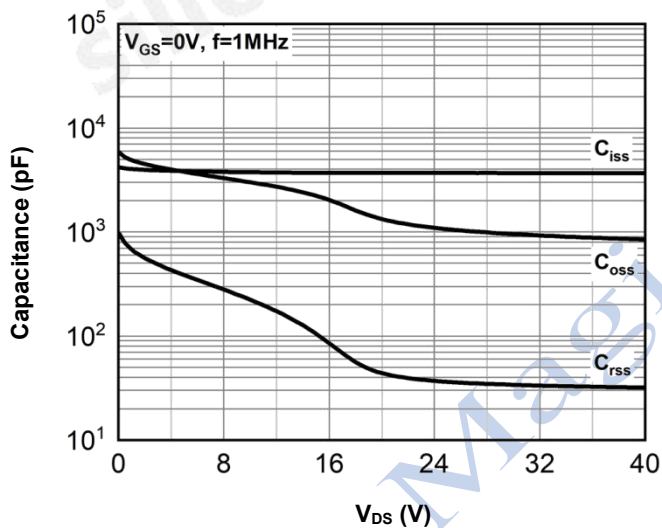


Fig.10 Single pulse maximum power dissipation

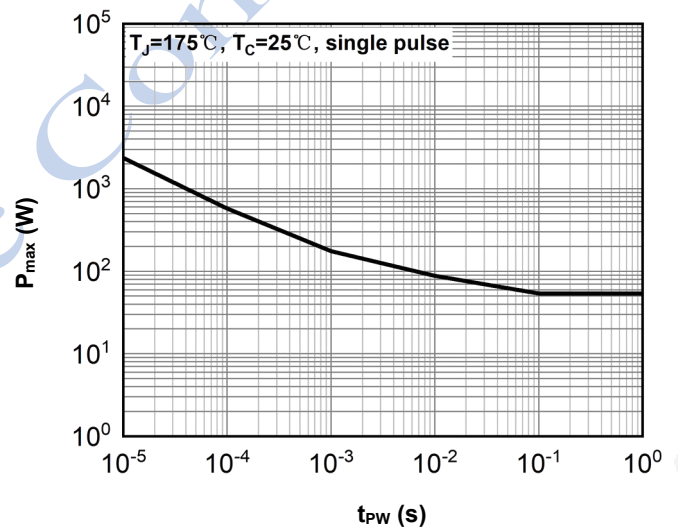


Fig.11 Max. power dissipation vs case temperature

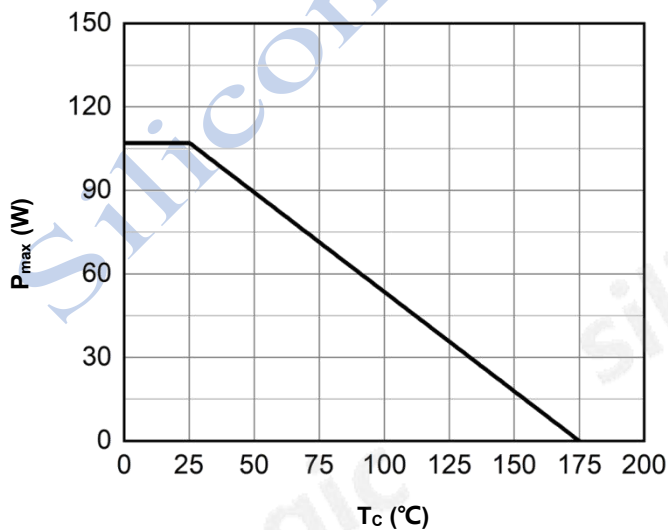


Fig.12 Max. continuous drain current vs case temperature

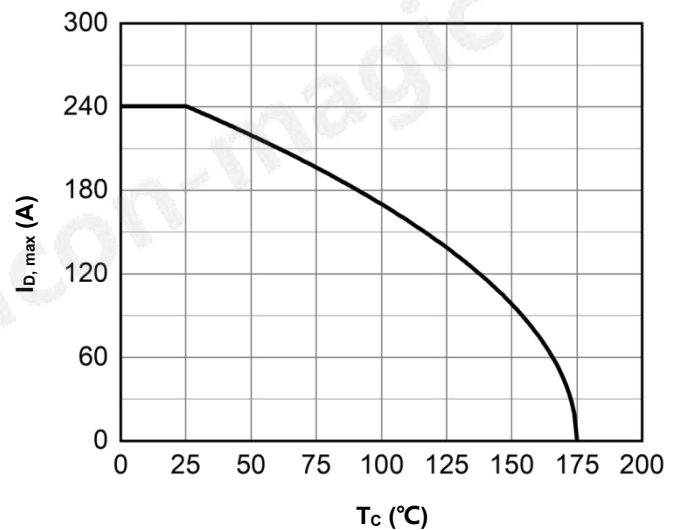


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

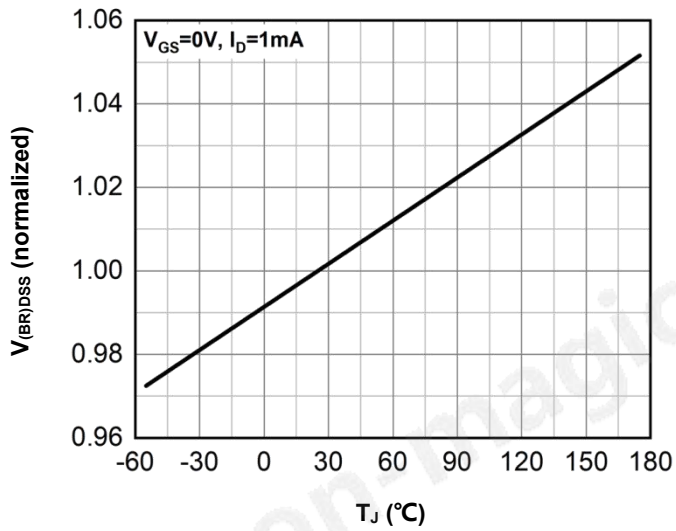


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

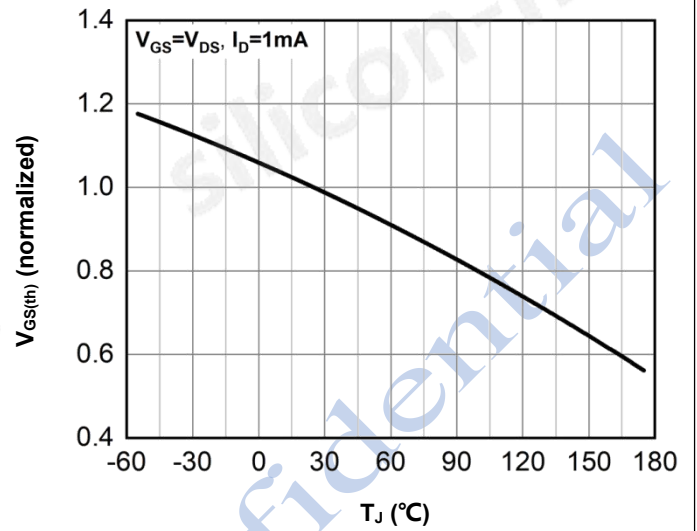
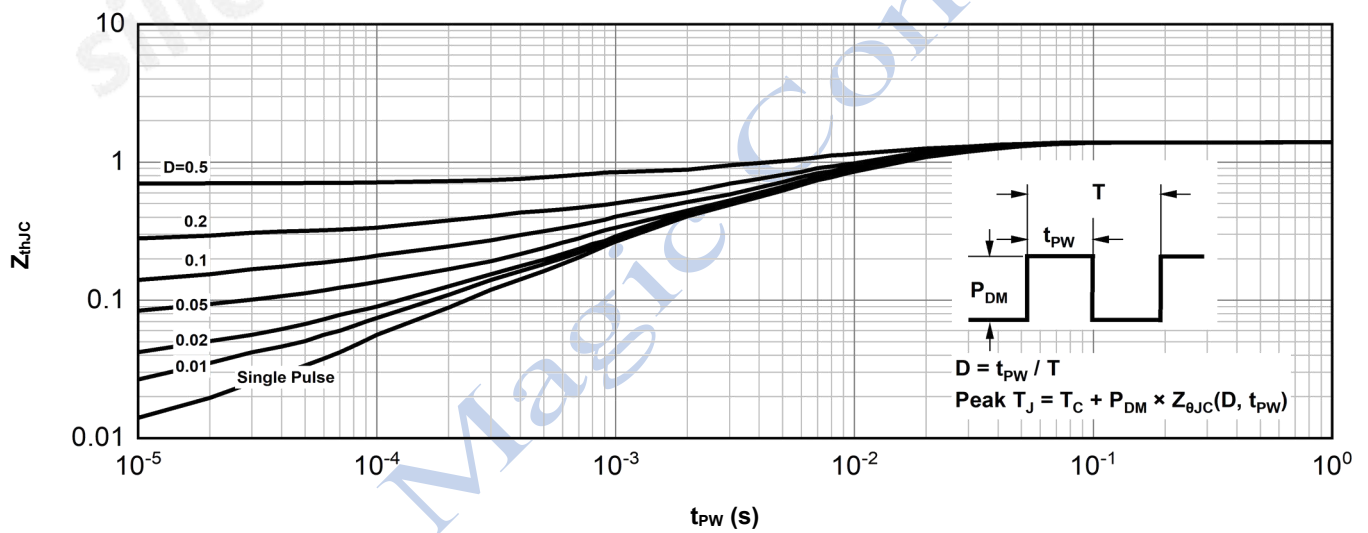
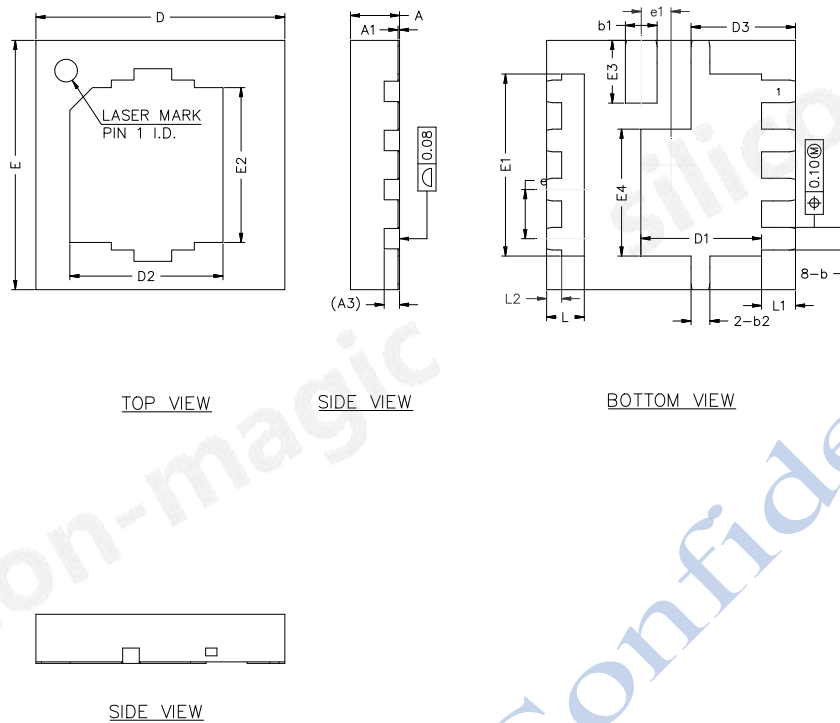


Fig.15 Transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	0.55	0.65	0.75
A1	0.00	0.02	0.05
A3	0.203 REF		
b	0.20	0.30	0.40
b1	0.32	0.42	0.52
b2	0.25 REF		
D	3.20	3.30	3.40
D1	1.50	1.60	1.70
D2	1.93	2.03	2.23
D3	1.28	1.38	1.48
E	3.20	3.30	3.40
E1	2.31	2.41	2.51
E2	1.95	2.05	2.25
E3	0.73	0.83	0.93
E4	1.58	1.68	1.78
e	0.55	0.65	0.75
e1	0.30	0.40	0.50
L	0.40	0.50	0.60
L1	0.35	0.45	0.55
L2	0.10	0.20	0.30

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