

Preliminary Specification: Subject to Change without Notice

N-Channel 80V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
80	1.1 @ $V_{GS} = 10V$	350 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- Motor drives

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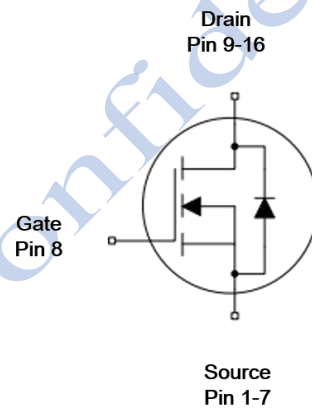
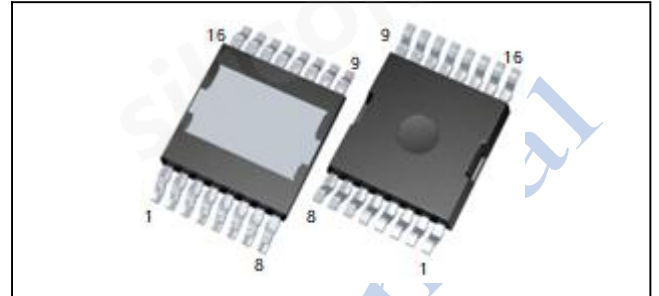
Package and ordering information

Ordering code	Package	Device code
SDH08N1P1QN-AA	TOLT	H08N1P1QN-AA

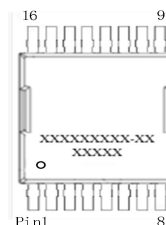
1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)				
Parameter		Symbol	Limit	Unit
Drain-source voltage		V_{DS}	80	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current	$T_C = 25^\circ\text{C}^{(1)}$	I_D	350	A
	$T_C = 100^\circ\text{C}^{(1)}$		296	
	$T_A = 25^\circ\text{C}^{(4)}$		34	
Pulsed drain current ⁽²⁾		$I_{D,pulse}$	1400	
Avalanche energy, single pulse ⁽³⁾		E_{AS}	1800	mJ
Power dissipation	$T_C = 25^\circ\text{C}$	P_D	375	W
	$T_A = 25^\circ\text{C}^{(4)}$		2.4	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

TOLT



RoHS
COMPLIANT
HALOGEN
FREE



XXXXXXXXXX-XX
Device code

XXXXXX
Lot number
Work week code
Year code

2. Thermal resistance ratings

Thermal resistance ratings					
Parameter		Symbol	Typ.	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.2	0.4	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$		62	

3. Electrical Characteristics

Electrical characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0, I_D = 250 \mu A$	80			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2.2	3	3.8	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10 \text{ V}, I_D = 100 \text{ A}$		1.0	1.1	m Ω
Forward transconductance ⁽⁵⁾	g_{fs}	$V_{DS} = 5 \text{ V}, I_D = 100 \text{ A}$		290		S
Gate resistance	R_g	$f = 1 \text{ MHz}$		3.2		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q_g	$V_{DS} = 40 \text{ V}, I_D = 50 \text{ A}, V_{GS} = 10 \text{ V}$		176		nC
Gate-source charge	Q_{gs}			65		
Gate-drain charge	Q_{gd}			29		
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 40 \text{ V}, I_D = 50 \text{ A}, V_{GS} = 10 \text{ V},$ $R_{GEN} = 6 \Omega$		141		ns
Rise time	t_r			95		
Turn-off delay time	$t_{d(off)}$			136		
Fall time	t_f			76		
Input capacitance	C_{iss}	$V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		13729		pF
Output capacitance	C_{oss}			2863		
Reverse transfer capacitance	C_{rss}			46		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0 \text{ V}, I_F = 50 \text{ A}$		0.9	1.2	V
Reverse recovery time	t_{rr}	$V_{DS} = 40 \text{ V}, I_F = 50 \text{ A}, di/dt = 100 \text{ A}/\mu s$		105		ns
Reverse recovery charge	Q_{rr}			236		nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 40 \text{ V}, V_{GS} = 10 \text{ V}, L = 0.1 \text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

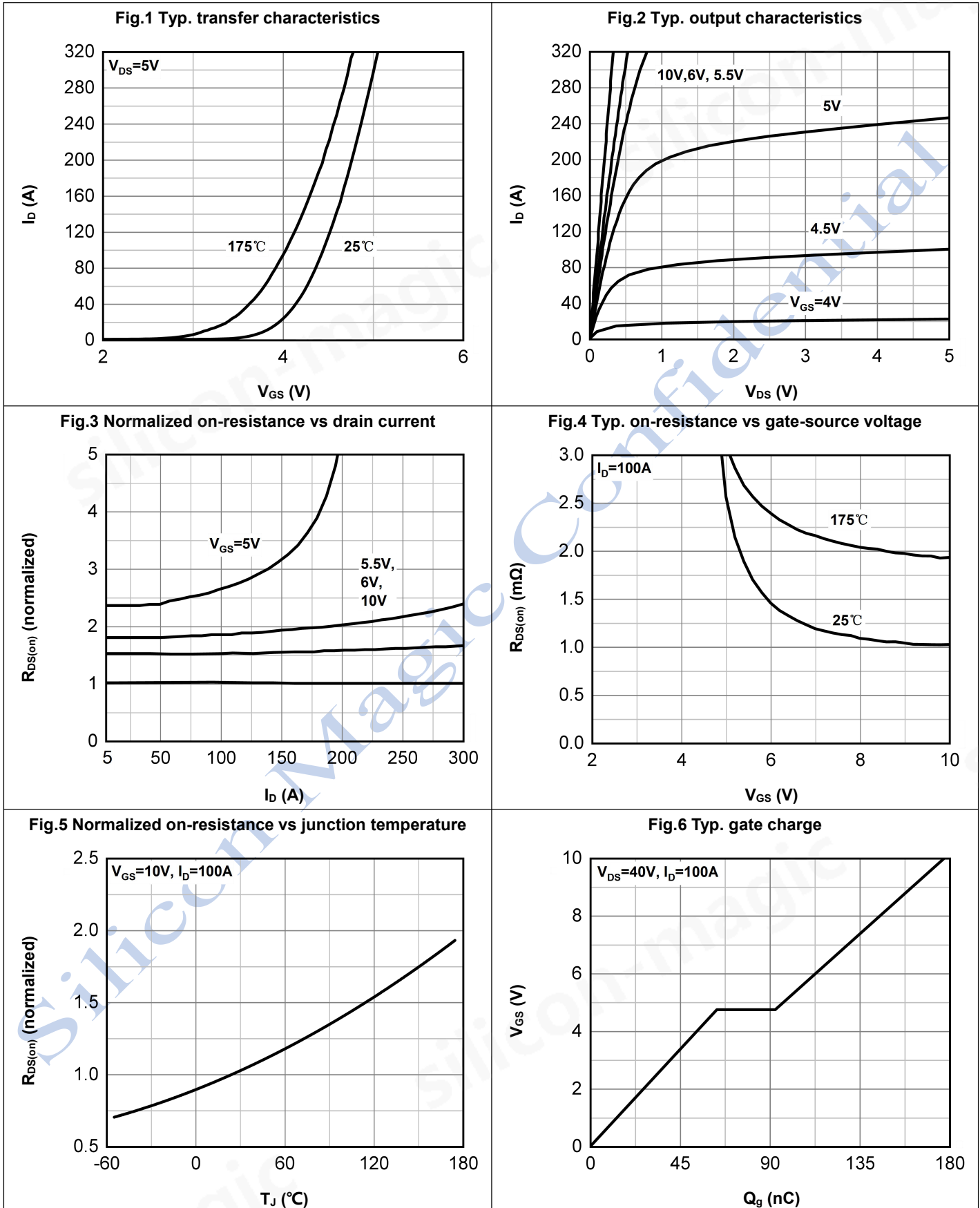


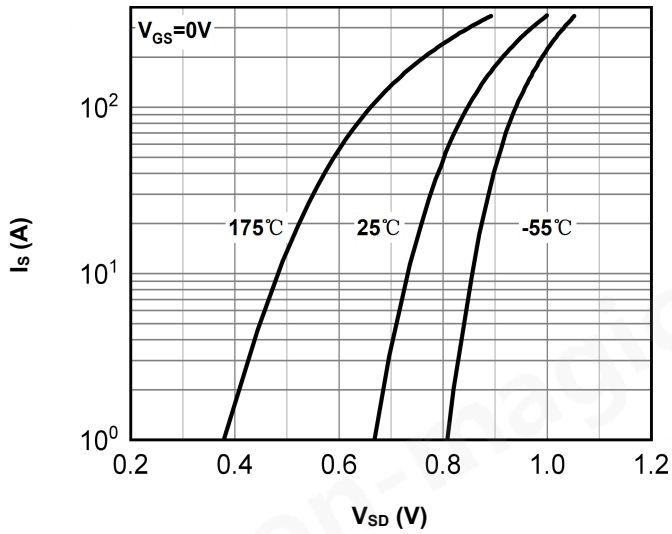
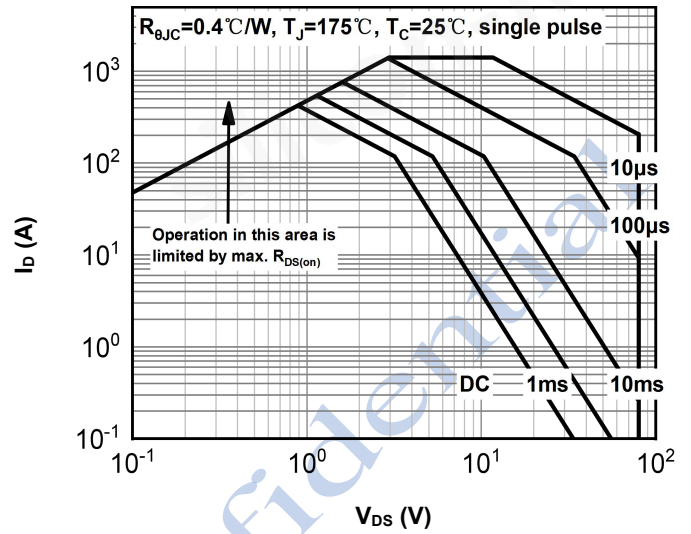
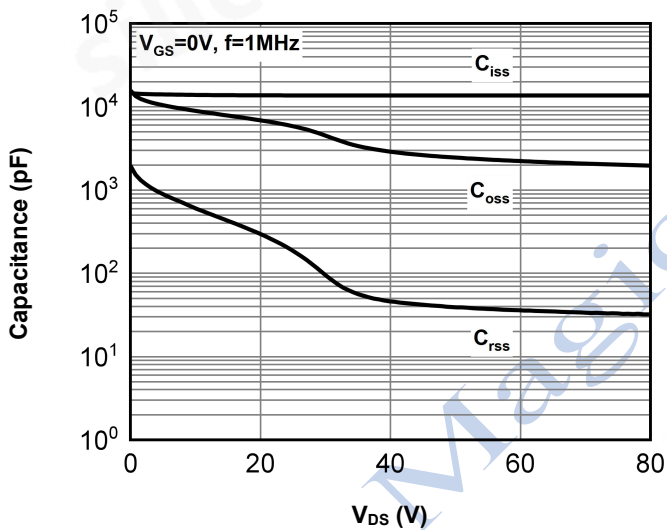
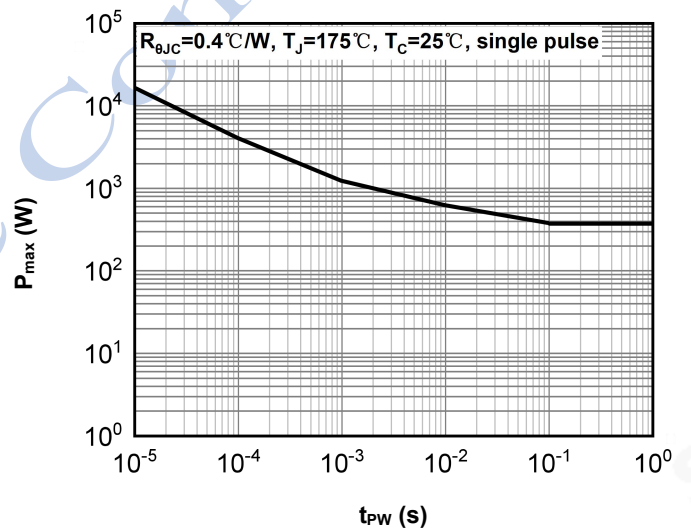
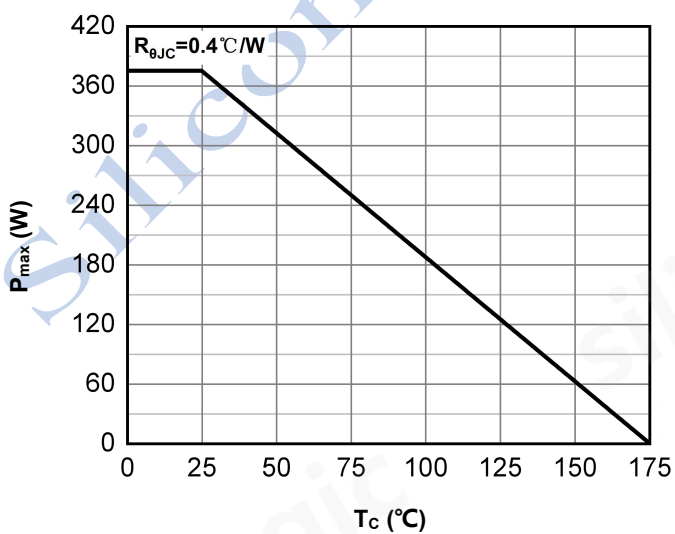
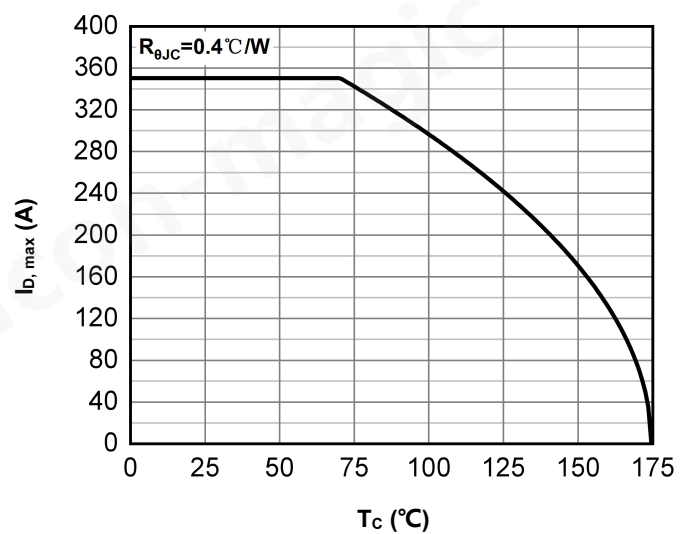
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

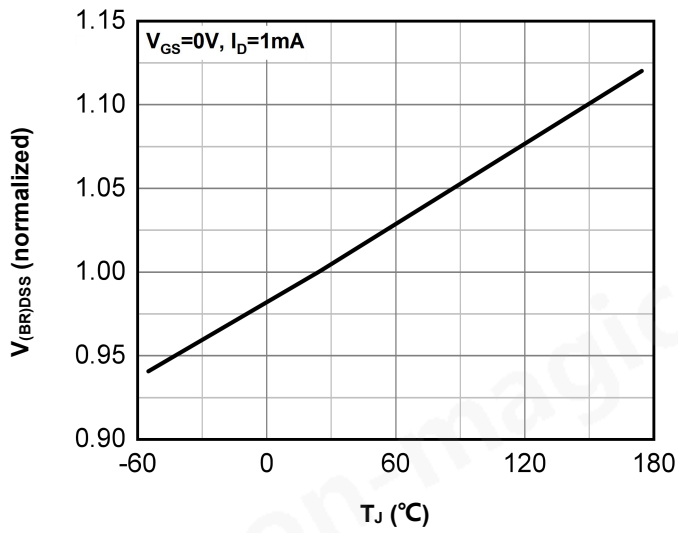


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

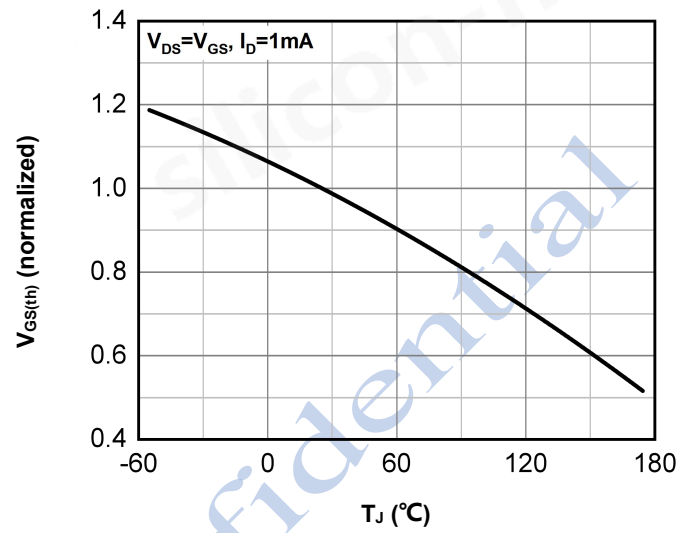
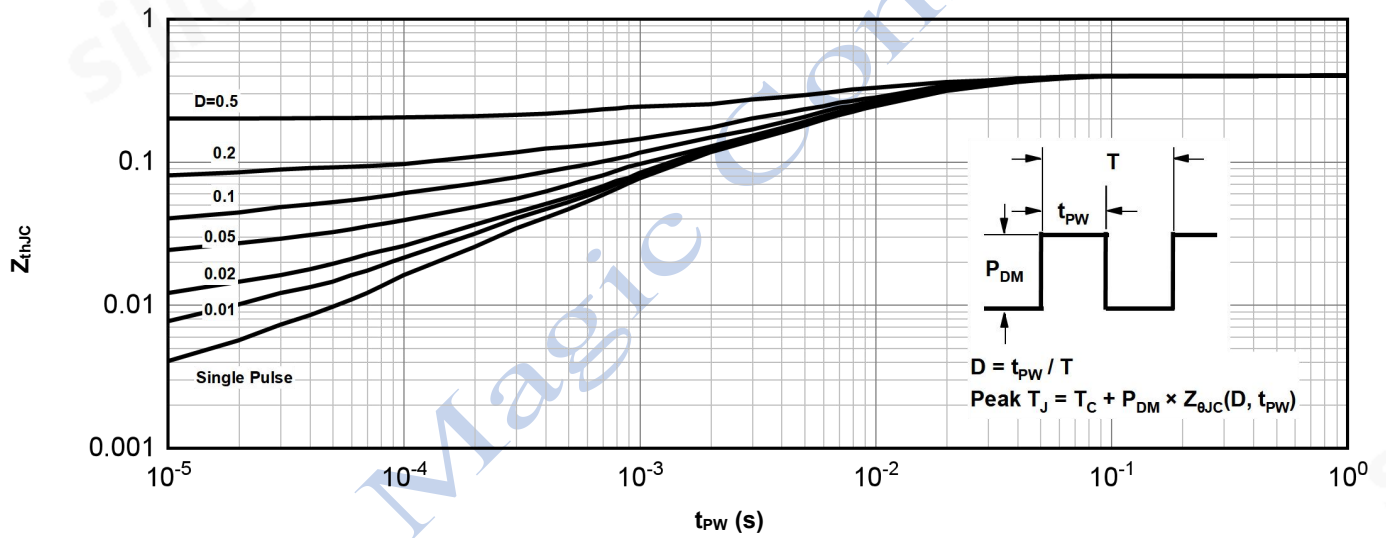
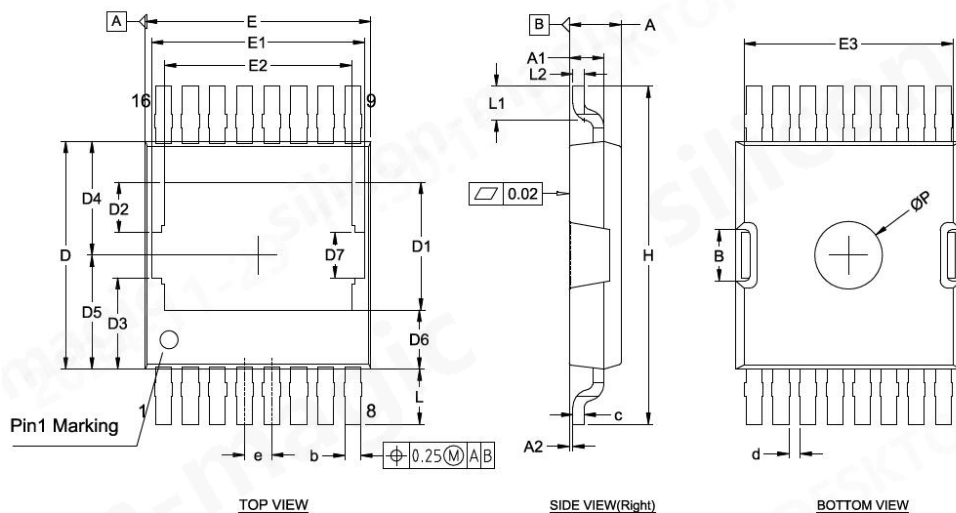


Fig.15 Transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	2.250	2.300	2.350
A1	1.440	1.540	1.640
A2	0.010	—	0.160
b	0.600	0.700	0.800
c	0.400	0.500	0.600
d	0.400	0.500	0.600
e	1.200 BSC		
D	10.000	10.100	10.300
D1	5.470	5.670	5.870
D2	2.040	2.240	2.440
D3	4.050 REF		
D4	5.050 REF		
D5	5.050 REF		
D6	2.620 REF		
D7	2.000 REF		
E	9.700	10.000	10.100
E1	9.460 REF		
E2	8.100	8.300	8.500
E3	9.070	9.270	9.470
H	14.800	15.000	15.200
L	2.250	2.450	2.650
L1	1.350	1.500	1.650
L2	0.500 BSC		
P	2.900	3.000	3.100
B	2.180	2.280	2.380

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