

Preliminary Specification: Subject to Change without Notice

N-Channel 80 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
80	1.49 @ $V_{GS} = 10V$	180 ⁽¹⁾

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

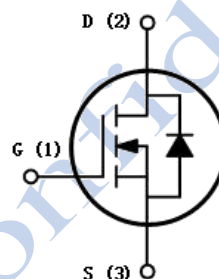
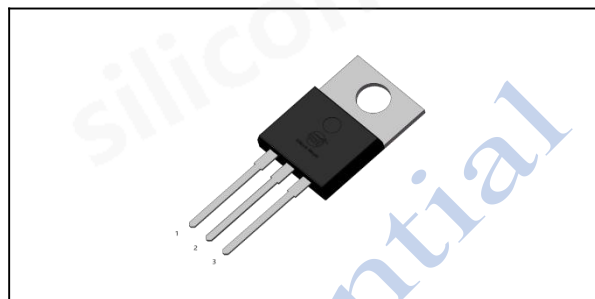
- DC/DC conversion
- Power switch
- Motor drives

 is the registered trademark of Silicon-Magic Semiconductor Technology (Hangzhou) Co., Ltd.

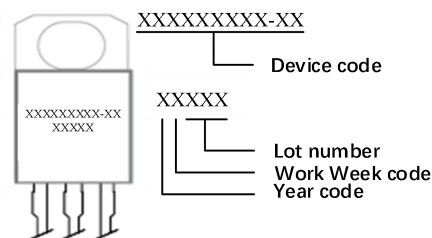
Package and ordering information

Ordering code	Package	Device code
SDH08N1P4AF-BT	TO220-3L	H08N1P4AF-BT

TO220-3L



RoHS
COMPLIANT
HALOGEN
FREE



1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	80	V
Gate-source voltage	V_{GS}	± 20	
Continuous drain current	$T_C = 25^\circ\text{C}$ ⁽¹⁾	180	A
	$T_C = 100^\circ\text{C}$	180	
	$T_A = 25^\circ\text{C}$ ⁽⁴⁾	36.1	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	720	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	1100	mJ
Power dissipation	$T_C = 25^\circ\text{C}$	375	W
	$T_A = 25^\circ\text{C}$ ⁽⁴⁾	3.7	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$

2. Thermal resistance ratings

Thermal resistance ratings				
Parameter		Symbol	Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.4	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	40	

3. Electrical Characteristics

Electrical characteristics (T _J = 25°C unless otherwise noted)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	2.2	3	3.8	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 80 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		1.3	1.49	mΩ
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 20 A		90		S
Gate resistance	R _g	f = 1 MHz		1.5		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 40 V, I _D = 20 A, V _{GS} = 10 V		139.9		nC
Gate-source charge	Q _{gs}			44.8		
Gate-drain charge	Q _{gd}			26.5		
Turn-on delay time	t _{d(on)}	V _{DS} = 40 V, I _D = 20 A, V _{GS} = 10 V, R _{GEN} = 1.6 Ω		37.4		ns
Rise time	t _r			32.5		
Turn-off delay time	t _{d(off)}			37.9		
Fall time	t _f			23.5		
Input capacitance	C _{iss}	V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz		10374		pF
Output capacitance	C _{oss}			3168		
Reverse transfer capacitance	C _{rss}			61		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 20 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 40 V, I _F = 20 A, di/dt = 100 A/μs		70		ns
Reverse recovery charge	Q _{rr}			105		nC

Notes

- (1) Package limited.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = v_{dshalf}\text{ V}, V_{GS} = 10\text{ V}, L = 0.1\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

Fig.1 Typ. transfer characteristics

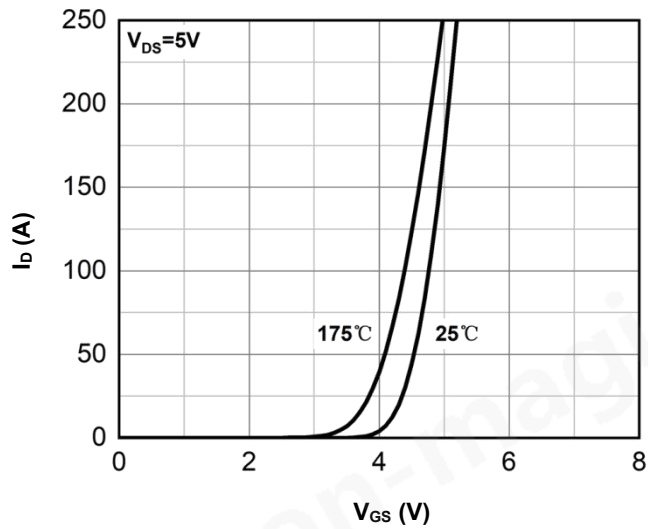


Fig.2 Typ. output characteristics

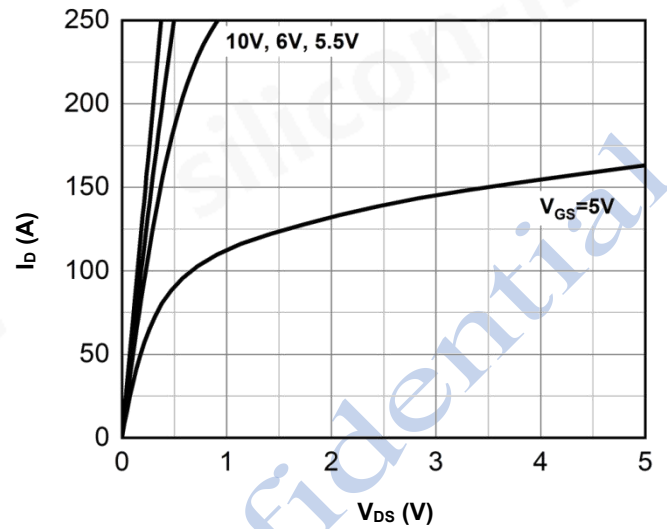


Fig.3 Normalized on-resistance vs drain current

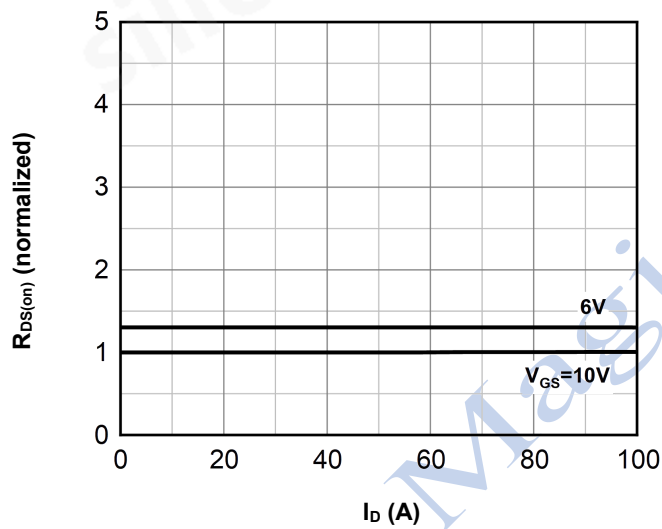


Fig.4 Typ. on-resistance vs gate-source voltage

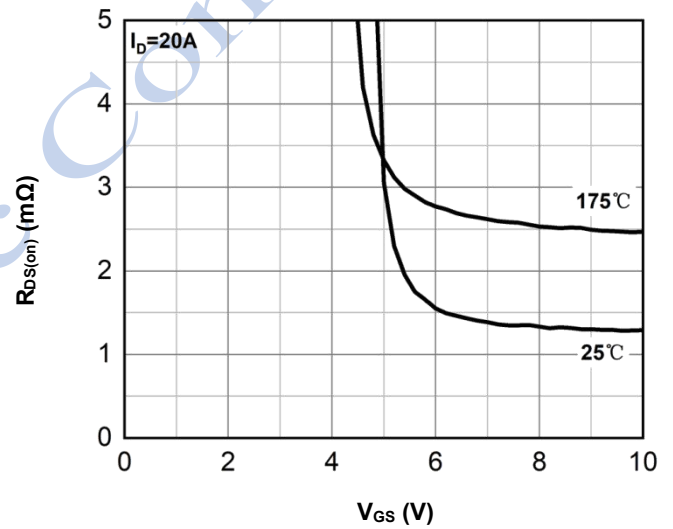


Fig.5 Normalized on-resistance vs junction temperature

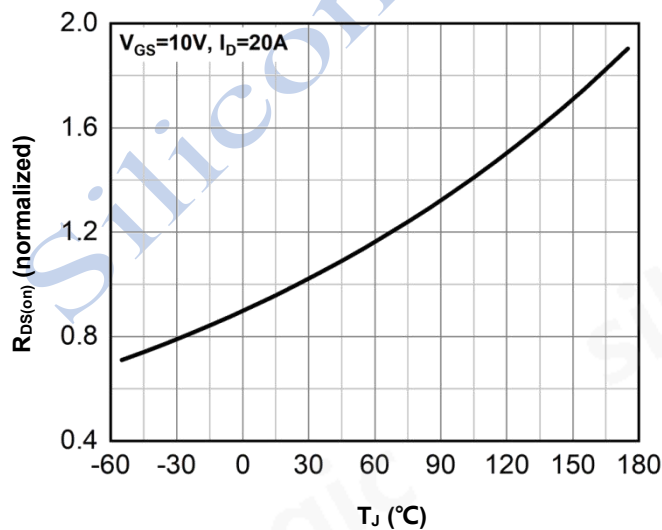


Fig.6 Typ. gate charge

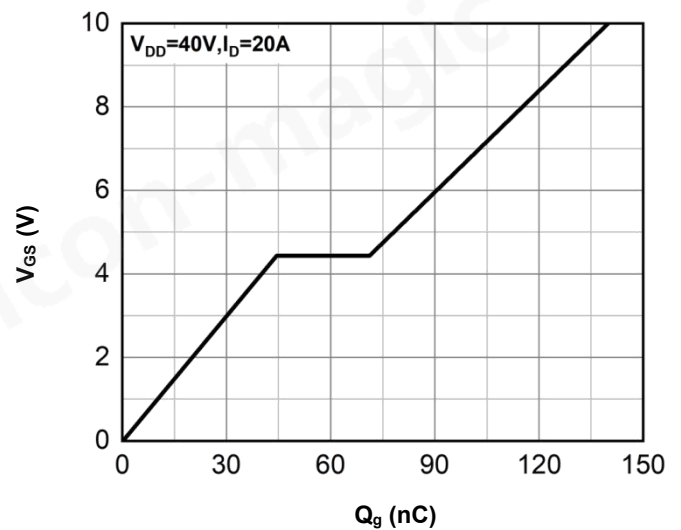


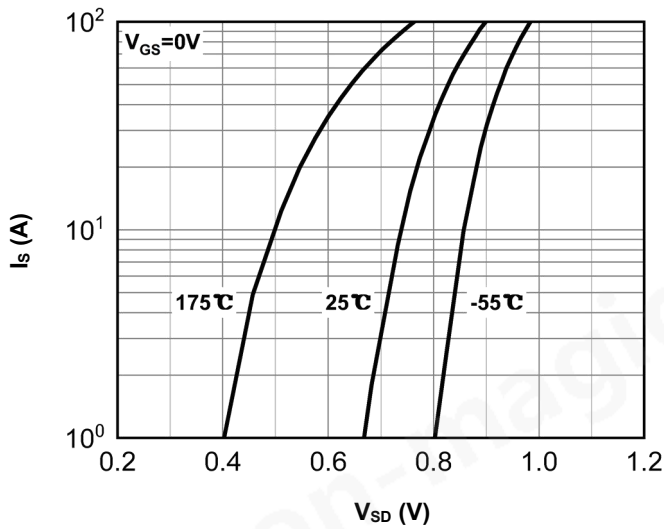
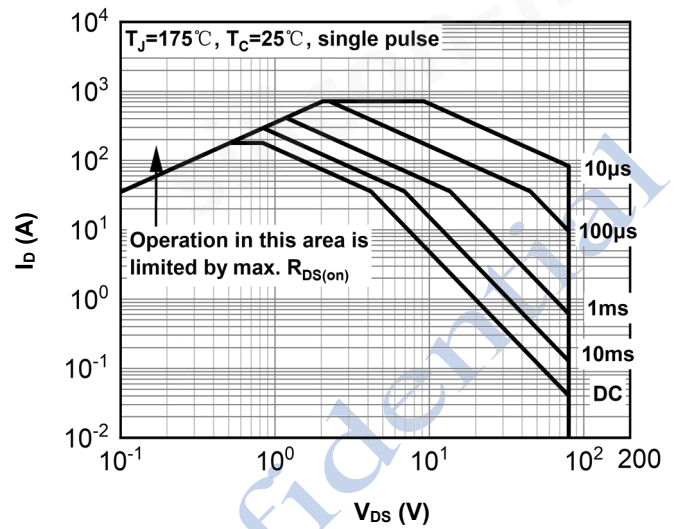
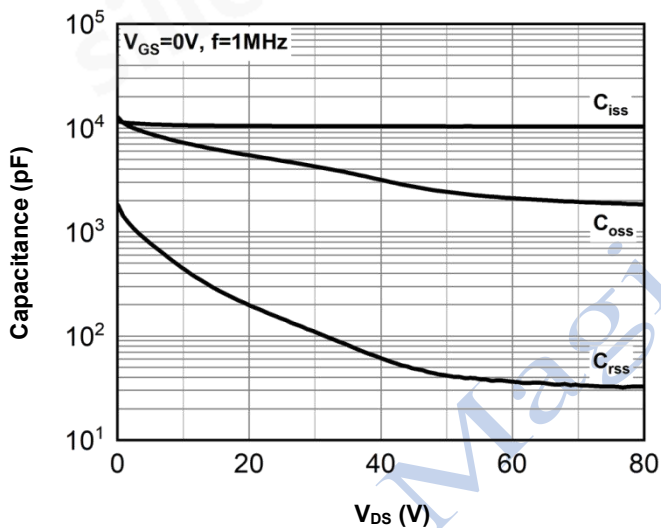
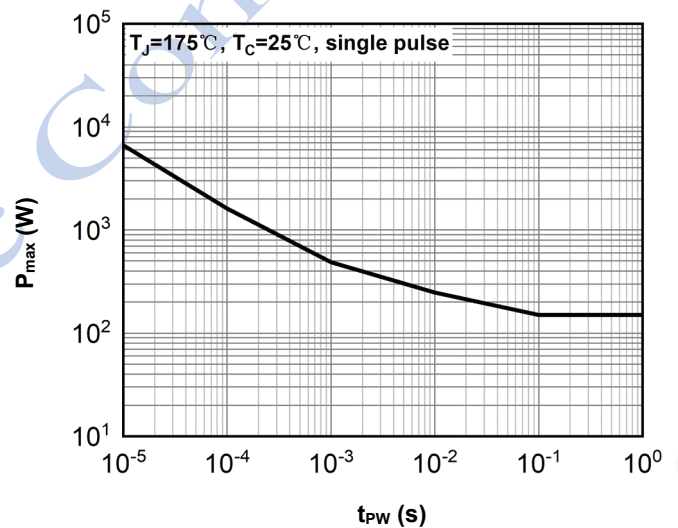
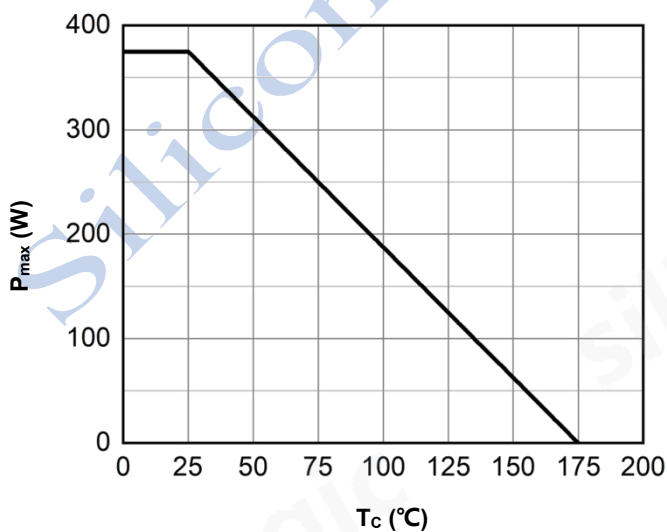
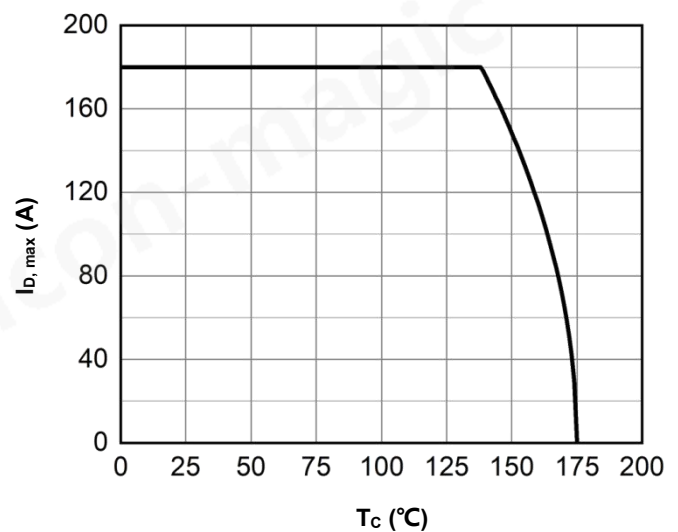
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

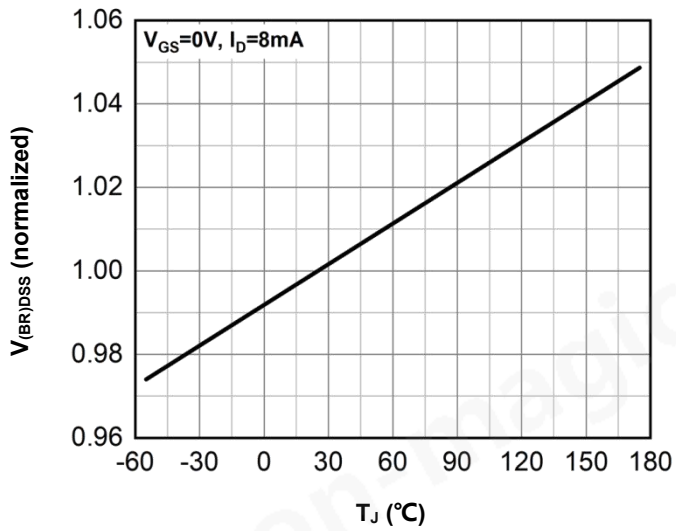


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

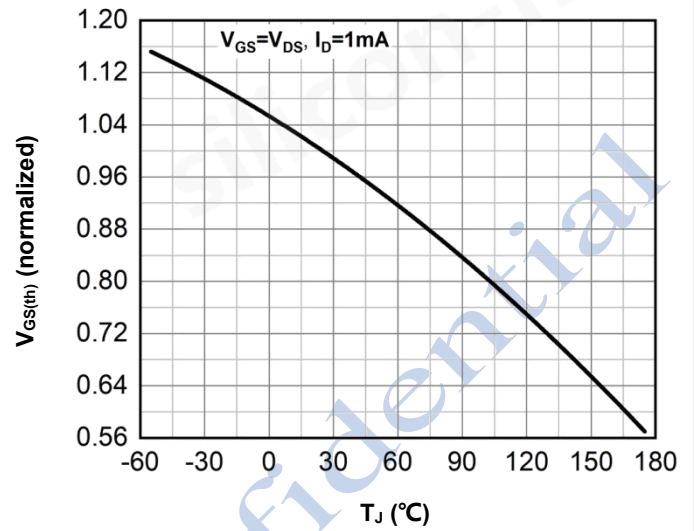
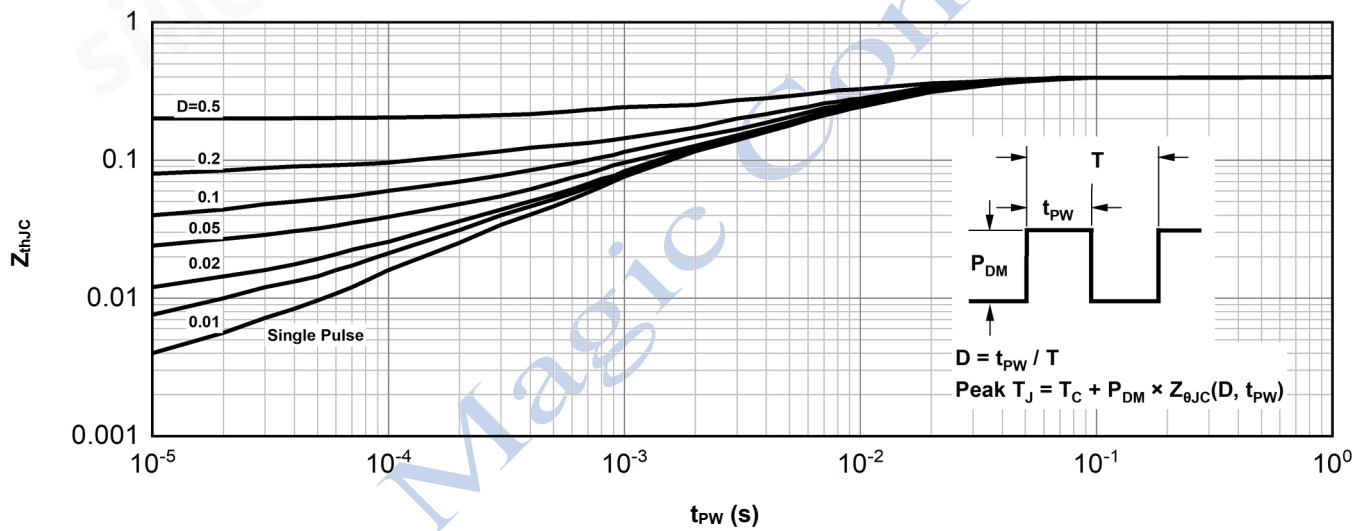
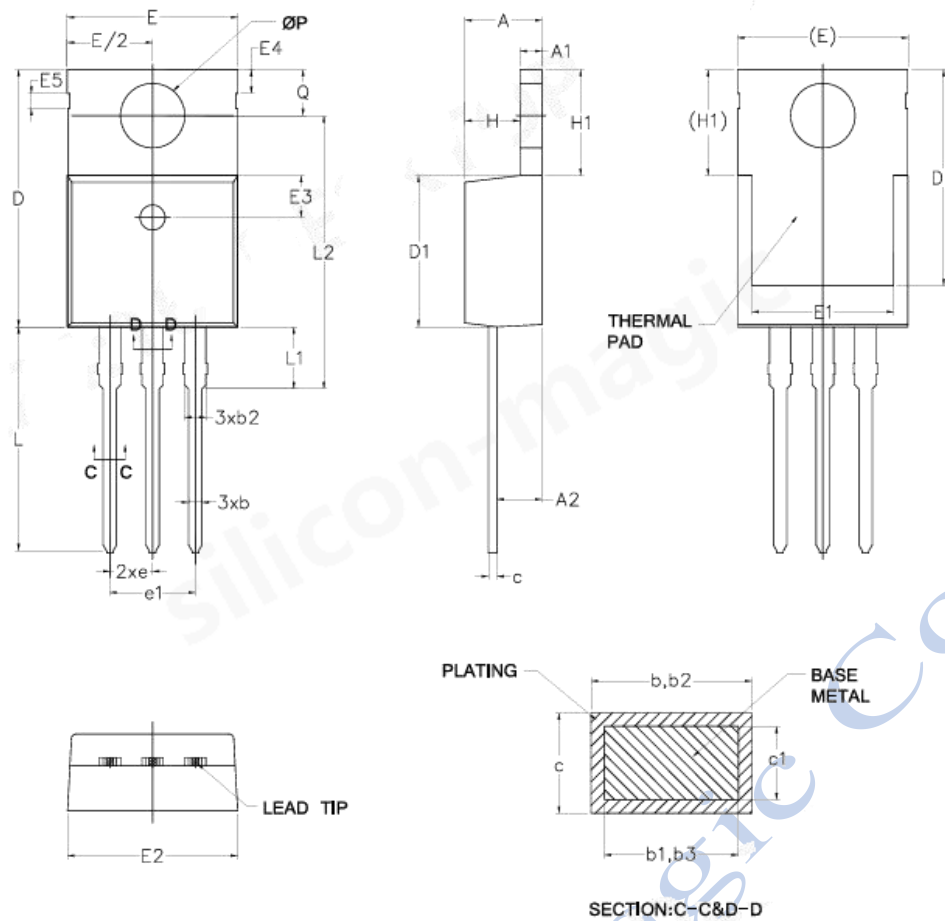


Fig.15 Transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	4.47	4.57	4.67
A1	1.20	1.30	1.40
A2	2.35	2.67	2.90
b	0.71	0.80	0.91
b1	0.71	0.80	0.86
b2	1.22	1.27	1.36
b3	1.22	1.27	1.31
c	0.47	0.50	0.60
c1	0.47	0.50	0.55
D	14.70	15.30	15.80
D1	8.90	9.00	9.47
D2	11.75	—	13.60
E	9.70	—	10.37
E1	7.00	8.44	8.89
E2	9.80	10.11	10.20
E3	2.40	2.50	2.60
E4	1.27	1.42	1.57
E5	0.90TYP		
e	2.54BSC		
e1	5.08BSC		
H	3.00	3.27	3.40
H1	6.15	6.30	6.45
L	12.90	13.45	14.80
L1	2.54	3.69	3.84
L2	12.13	16.25	16.50
P	3.60	3.84	3.90
Q	2.65	2.74	2.95

Legal Disclaimer

The information given in this document shall be for illustrative purposes only and shall in no event be regarded as a guarantee of conditions or characteristics. Silicon Magic Technologies reserves the right to change any information herein. With respect to any examples, hints or any typical values stated herein and/or any information regarding the application of the product, Silicon Magic Technologies or its affiliates hereby make no representation or warranty of any kind, expressed or implied, as to any information provided hereunder, including without limitation as to the accuracy, completeness or non-infringement of intellectual property rights of any third party, and they assume no liability for the consequences of use of such information. In addition, any information given in this document is subject to customer's compliance with its obligations stated herein and any applicable legal requirements, norms and standards concerning customer's products and any use of the product of Silicon Magic Technologies in customer's applications. The information contained herein is exclusively intended for technically trained staff. No license is granted by implication under any patent right, copyright, mask work right, or other intellectual property right. It is customer's sole responsibility to evaluate the suitability of the product for the intended application and the completeness of the product information given herein with respect to such application. In no event shall Silicon Magic Technologies or its affiliates be liable to any party for any direct, indirect, special, punitive, incidental or consequential damages of any nature whatsoever, including but not limited to loss of profits and loss of goodwill, whether or not such damages are based on tort or negligence, warranty, breach of contract or any other legal theory. In addition, any recipient of this document and the relevant products samples may not alter, decompile, disassemble, reverse engineer, or otherwise modify any information/samples received hereunder. Any intellectual property rights arising from the reverse engineering of Silicon Magic's products shall belong to Silicon Magic.