Preliminary Specification: Subject to Change without Notice

N-Channel 100 V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
100	1.9 @ V_{GS} = 10V	270 (1)

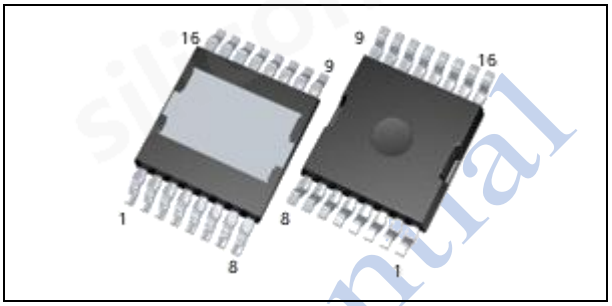
Features

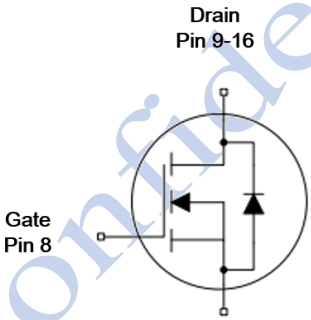
- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

- DC/DC conversion
- Power switch
- Motor drives

TOLT





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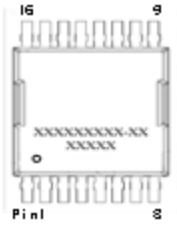
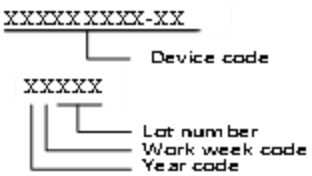




Package and ordering information

Ordering code	Package	Device code
SDH10N1P9QC-AA	TOLT	H10N1P9QC-AA

1. Maximum ratings

Absolute maximum ratings (T_A = 25℃ unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-source voltage		V_{DS}	100	V
Gate-source voltage		V_{GS}	±20	
Continuous drain current	T_C=25℃ (1)	I_D	270	A
	T_C=100℃		170	
	T_A=25℃ (4)		30	
Pulsed drain current(2)		$I_{D,pulse}$	1080	
Avalanche energy, single pulse(3)		E_{AS}	420	mJ
Power dissipation	T_C=25℃	P_D	250	W
	T_A=25℃ (4)		3.1	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 150	℃

2. Thermal resistance ratings

Thermal resistance ratings				
Parameter		**Symbol**	**Max.**	**Unit**
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.5	℃/W
Thermal resistance, junction-to-ambient (4)	Steady state	$R_{\theta JA}$	40	

3. Electrical Characteristics

Electrical characteristics (T_J = 25℃ unless otherwise noted)						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 1 mA	100			V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.2	3	3.8	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V			1	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 60 A		1.6	1.9	mΩ
Forward transconductance(5)	g_{fs}	V_{DS} = 5 V, I_D = 60 A		190		S
Gate resistance	R_g	f = 1 MHz		2.9		Ω
Dynamic(5)						
Total gate charge	Q_g	V_{DS} = 50 V, I_D = 60 A, V_{GS} = 10 V		129		nC
Gate-source charge	Q_{gs}			54.8		
Gate-drain charge	Q_{gd}			18.9		
Turn-on delay time	$t_{d(on)}$	V_{DS} = 50 V, I_D = 60 A, V_{GS} = 10 V, R_{GEN} = 1.6 Ω		61.4		ns
Rise time	t_r			34.1		
Turn-off delay time	$t_{d(off)}$			34.3		
Fall time	t_f			18.6		
Input capacitance	C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz		10492		pF
Output capacitance	C_{oss}			2361		
Reverse transfer capacitance	C_{rss}			45		
Reverse Diode Characteristics(5)						
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 60 A		0.9	1.1	V
Reverse recovery time	t_{rr}	V_{DS} = 50 V, I_F = 60 A, di/dt = 100 A/μs		87		ns
Reverse recovery charge	Q_{rr}			200		nC

Notes

(1) Package limited.

(2) Pulse width limited by maximum junction temperature.

(3) V_{DS} = 50 V, V_{GS} = 10 V, L = 1 mH.

(4) $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.

(5) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

Fig.1 Typ. transfer characteristics

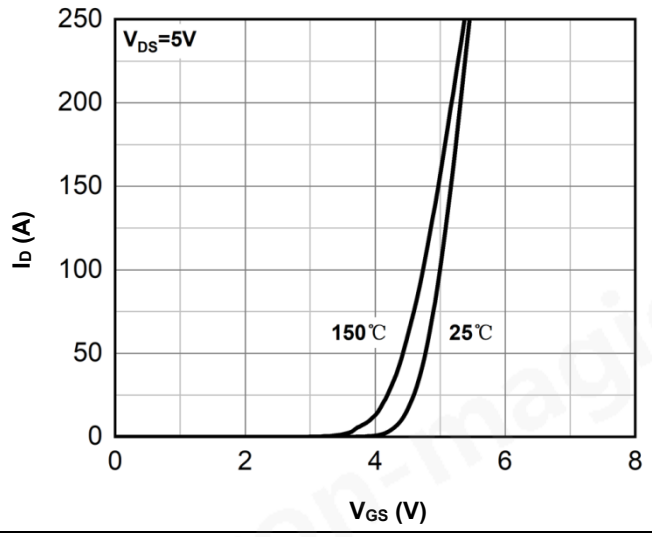


Fig.2 Typ. output characteristics

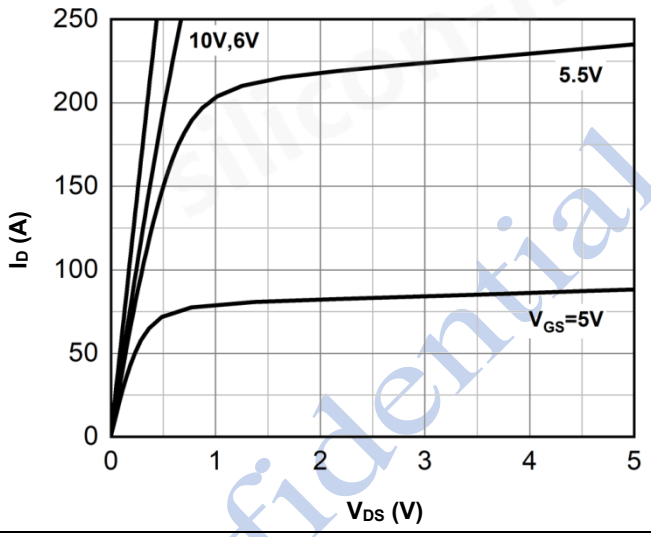


Fig.3 Normalized on-resistance vs drain current

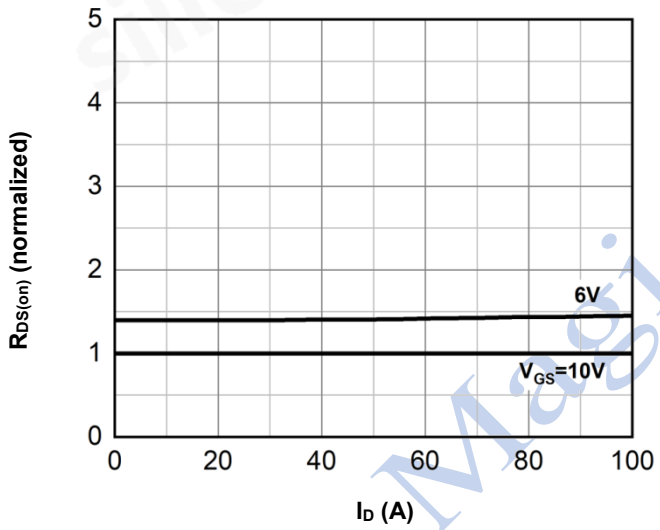


Fig.4 Typ. on-resistance vs gate-source voltage

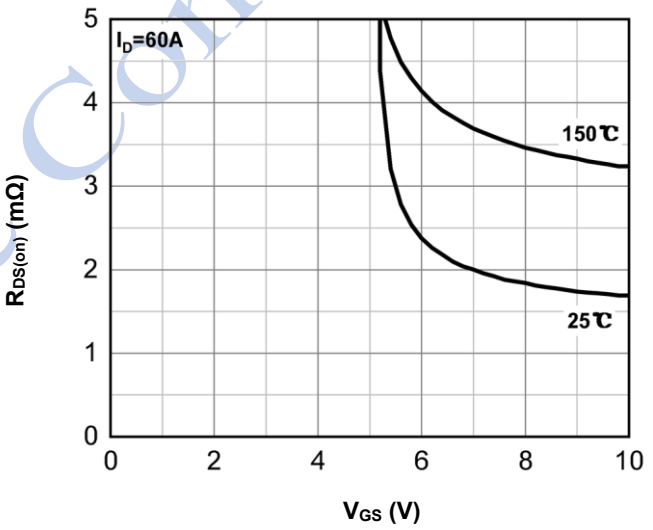


Fig.5 Normalized on-resistance vs junction temperature

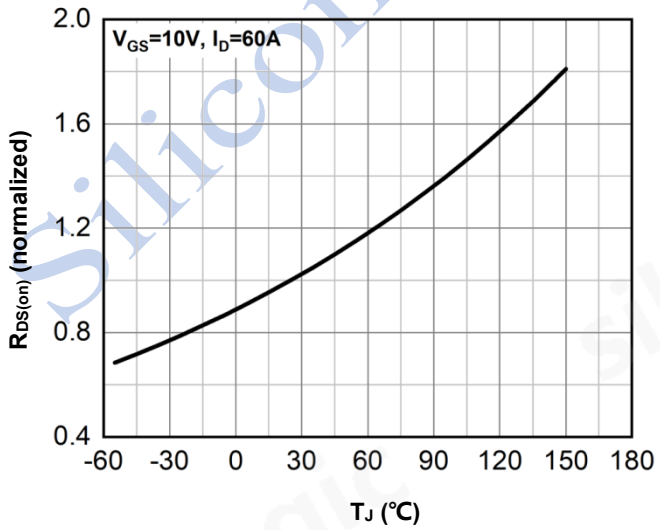


Fig.6 Typ. gate charge

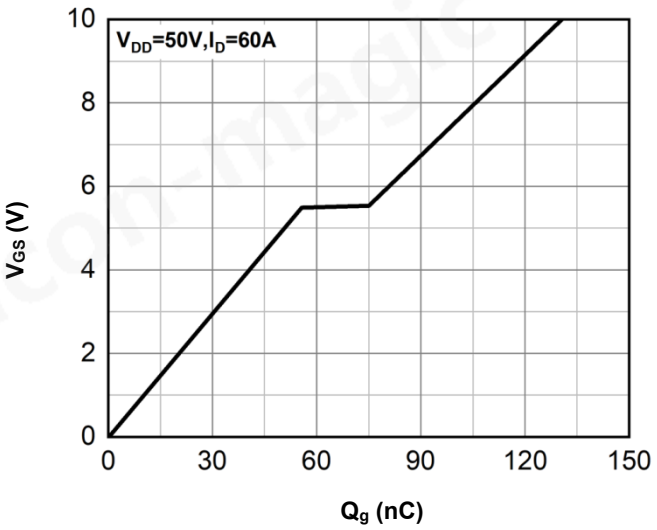


Fig.7 Typ. forward characteristics of body diode

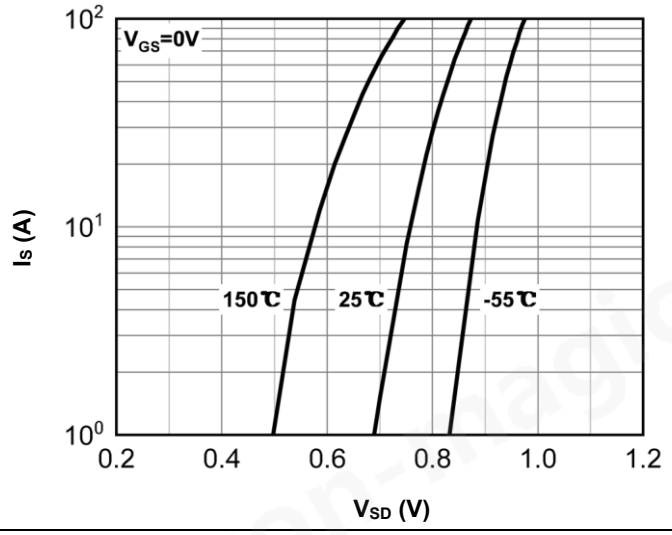


Fig.8 Safe operating area

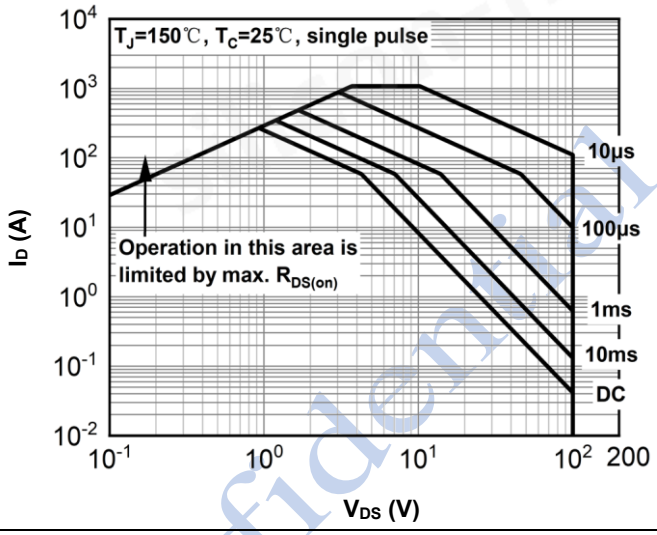


Fig.9 Typ. Capacitance

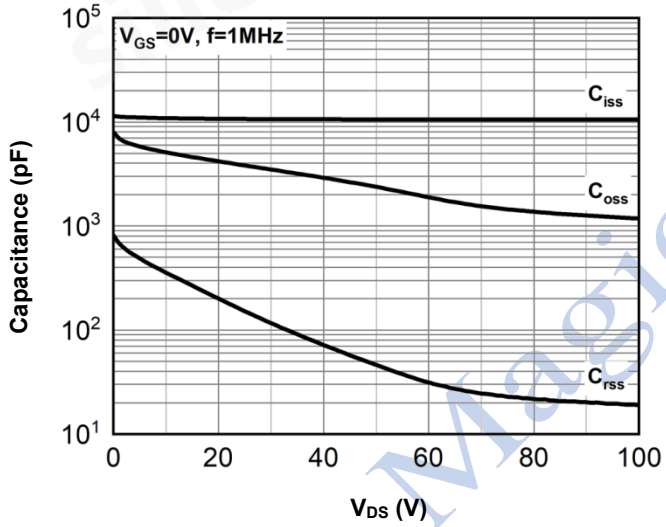


Fig.10 Single pulse maximum power dissipation

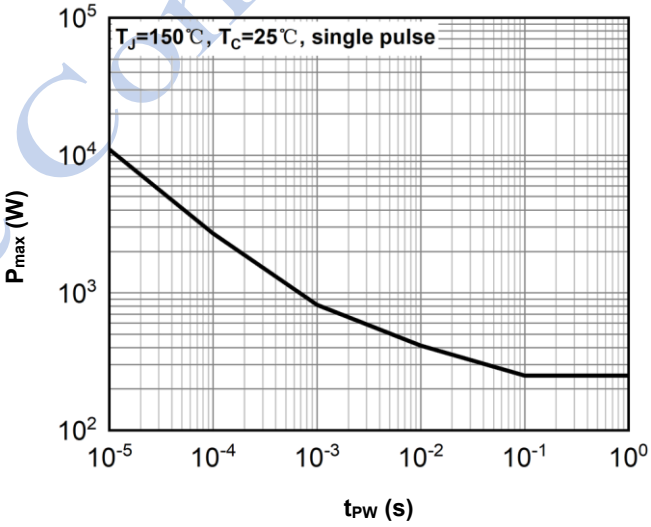


Fig.11 Max. power dissipation vs case temperature

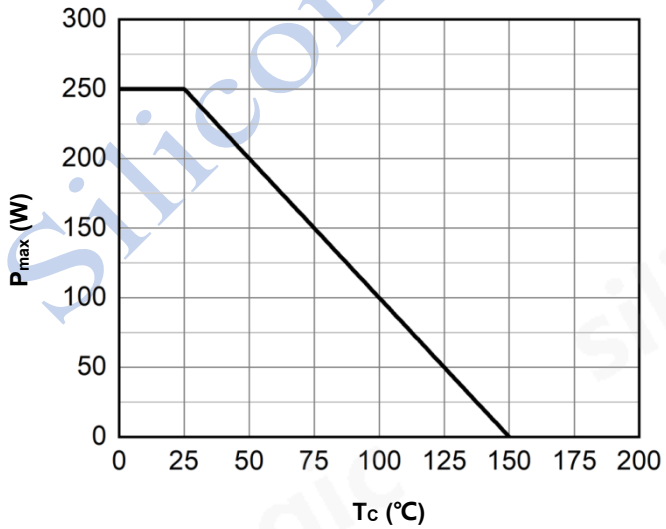


Fig.12 Max. continuous drain current vs case temperature

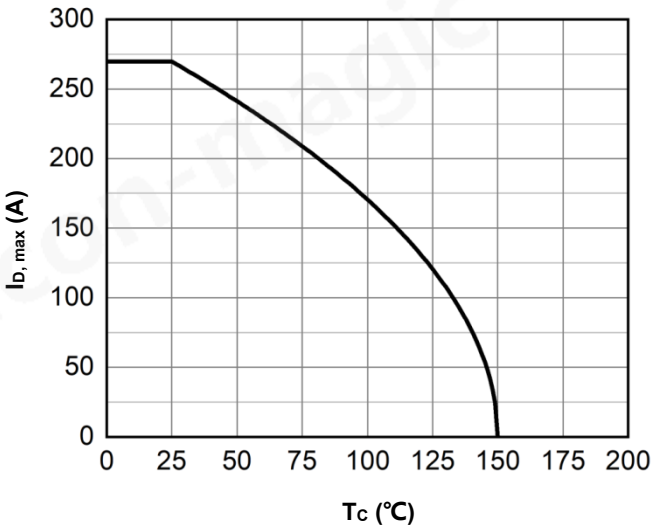


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

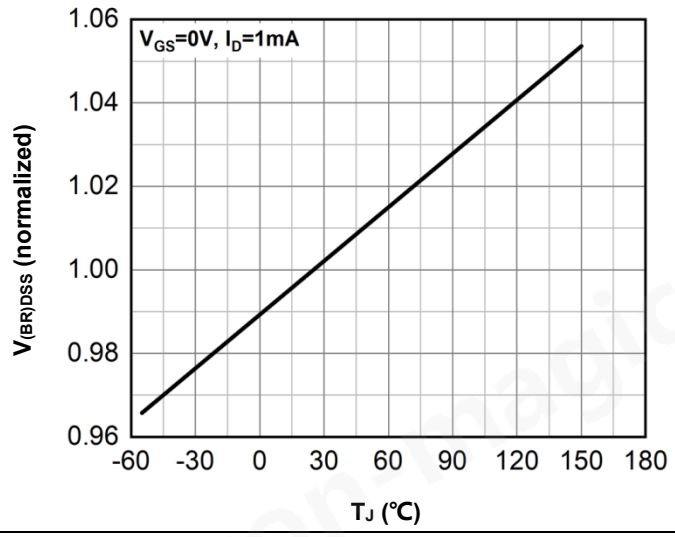


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

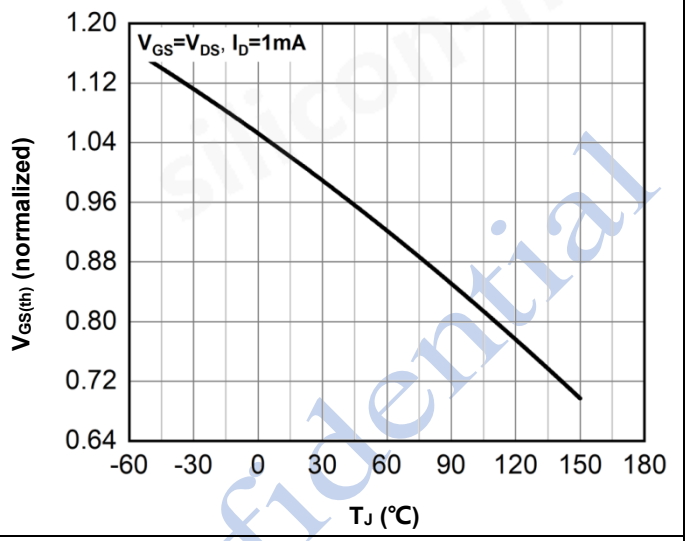
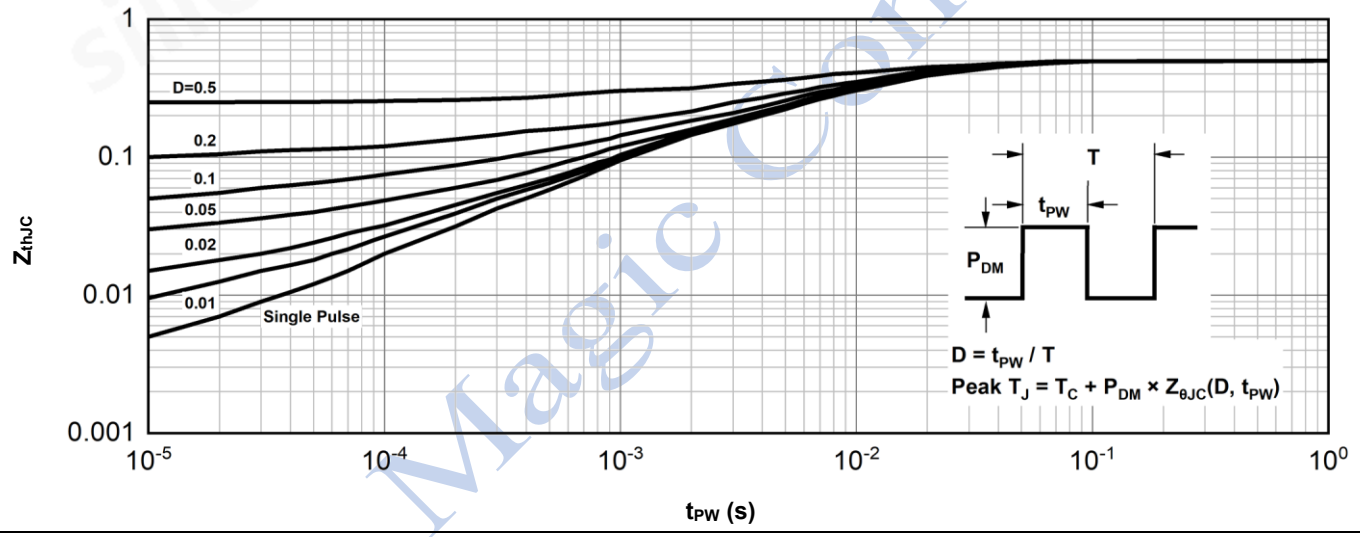
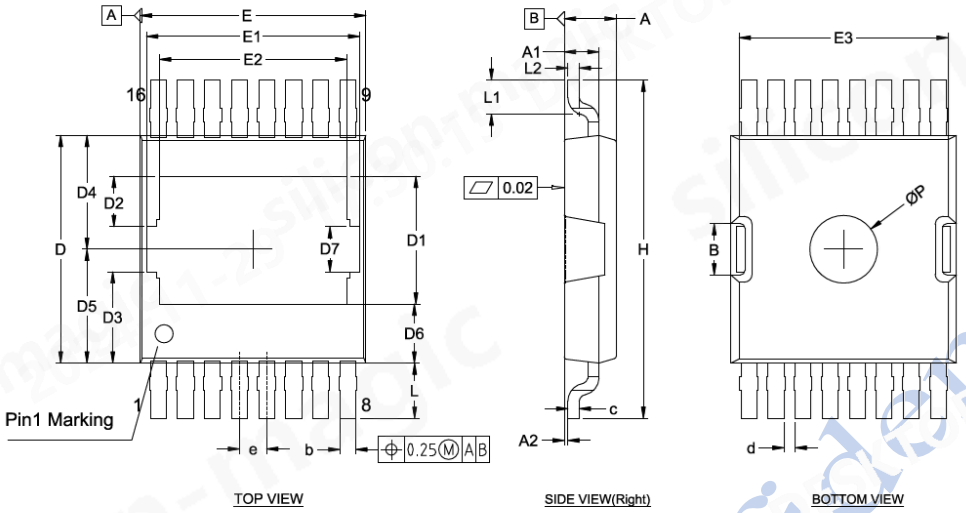


Fig.15 Transient thermal impedance from junction to case



5. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	2.250	2.300	2.350
A1	1.440	1.540	1.640
A2	0.010	—	0.160
b	0.600	0.700	0.800
c	0.400	0.500	0.600
d	0.400	0.500	0.600
e	1.200 BSC		
D	10.000	10.100	10.300
D1	5.470	5.670	5.870
D2	2.040	2.240	2.440
D3	4.050 REF		
D4	5.050 REF		
D5	5.050 REF		
D6	2.620 REF		
D7	2.000 REF		
E	9.700	10.000	10.100
E1	9.460 REF		
E2	8.100	8.300	8.500
E3	9.070	9.270	9.470
H	14.800	15.000	15.200
L	2.250	2.450	2.650
L1	1.350	1.500	1.650
L2	0.500 BSC		
P	2.900	3.000	3.100
B	2.180	2.280	2.380

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