

Preliminary Specification: Subject to Change without Notice

Dual Asymmetric N-Channel 30 V MOSFET

Product summary

	V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
Q1	30	5.5 @ $V_{GS} = 10V$	40 ⁽¹⁾
		7.2 @ $V_{GS} = 4.5V$	
Q2	30	2.3 @ $V_{GS} = 10V$	80 ⁽¹⁾
		2.8 @ $V_{GS} = 4.5V$	

Features

- Low $R_{DS(on)}$ SGT technology
- Low thermal impedance
- Fast switching speed
- 100% avalanche tested

Applications

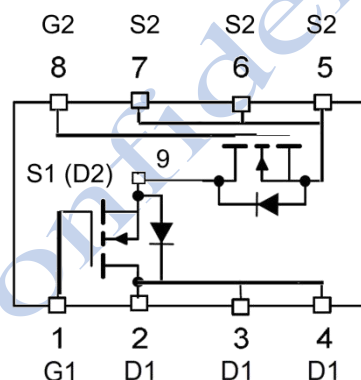
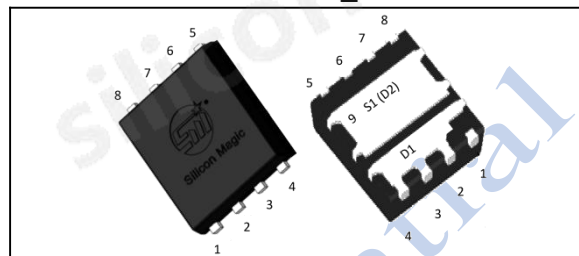
- DC/DC conversion
- Power switch
- Motor drives

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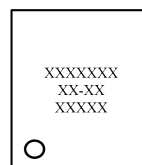
Package and ordering information

Ordering code	Package	Device code
SMN03L2P5NN-AA	PDFN5*6-D_A1	N03L2P5NN-AA

PDFN5*6-D_A1



RoHS
COMPLIANT
HALOGEN
FREE



XXXXXX
XX-XX
XXXXX
Device code
lot number
Work week code
Year code

1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Q1 Limit	Q2 Limit	Unit
Drain-source voltage	V_{DS}	30	30	V
Gate-source voltage	V_{GS}	± 20	± 12	
Continuous drain current	I_D	56	110	A
		40	80	
		14.5	23.1	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	160	320	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	22	90	mJ
Power dissipation	P_D	50	83.3	W
		1.9	2	
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	-55 to 150	$^\circ\text{C}$

2. Thermal resistance ratings

Thermal resistance ratings					
Parameter		Symbol	Q1 Max.	Q2 Max.	Unit
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	2.5	1.5	°C/W
Thermal resistance, junction-to-ambient ⁽⁴⁾	Steady state	$R_{\theta JA}$	65	60	

3. Q1 Electrical Characteristics

Electrical characteristics (T _J = 25°C unless otherwise noted)						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 1 mA	30			V
Gate-source threshold voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 1 mA	1.0	1.6	2.2	V
Gate-body leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero gate voltage drain current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
Drain-source on-resistance	R _{DS(on)}	V _{GS} = 10 V, I _D = 20 A		4.6	5.5	mΩ
		V _{GS} = 4.5 V, I _D = 10 A		6.0	7.2	
Forward transconductance ⁽⁵⁾	g _{fs}	V _{DS} = 5 V, I _D = 20 A		61		S
Gate resistance	R _g	f = 1 MHz		1.1		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q _g	V _{DS} = 15 V, I _D = 10 A, V _{GS} = 4.5 V		5.8		nC
Total gate charge	Q _g	V _{DS} = 15 V, I _D = 20 A, V _{GS} = 10 V		12.4		nC
Gate-source charge	Q _{gs}			2.7		
Gate-drain charge	Q _{gd}			2.1		
Turn-on delay time	t _{d(on)}	V _{DS} = 15 V, I _D = 20 A, V _{GS} = 10 V, R _{GEN} = 1.6 Ω		1.8		ns
Rise time	t _r			1.8		
Turn-off delay time	t _{d(off)}			4.6		
Fall time	t _f			2.3		
Input capacitance	C _{iss}	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz		947		pF
Output capacitance	C _{oss}			388		
Reverse transfer capacitance	C _{rss}			16		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V _{SD}	V _{GS} = 0 V, I _F = 20 A		0.8	1.1	V
Reverse recovery time	t _{rr}	V _{DS} = 15 V, I _F = 20 A, di/dt = 100 A/μs		22		ns
Reverse recovery charge	Q _{rr}			11		nC

Notes

- (1) Silicon limited. (The package-limited current is 40 A for Q1 and 80 A for Q2 respectively)
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 15\text{ V}, V_{GS} = 10\text{ V}, L = 1\text{ mH}$.
- (4) $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5x1.5 in. board of FR-4 material.
- (5) Guaranteed by design, not subject to production testing.

4. Q2 Electrical Characteristics

Electrical characteristics ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	30			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	1.0	1.6	2.2	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 12\text{ V}$			± 100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 40\text{ A}$		1.8	2.3	m Ω
		$V_{GS} = 4.5\text{ V}, I_D = 20\text{ A}$		2.2	2.8	
Forward transconductance ⁽⁵⁾	g_{fs}	$V_{DS} = 5\text{ V}, I_D = 40\text{ A}$		203		S
Gate resistance	R_g	$f = 1\text{ MHz}$		1.4		Ω
Dynamic ⁽⁵⁾						
Total gate charge	Q_g	$V_{DS} = 15\text{ V}, I_D = 20\text{ A}, V_{GS} = 4.5\text{ V}$		23.2		nC
Total gate charge	Q_g	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}, V_{GS} = 10\text{ V}$		51.9		nC
Gate-source charge	Q_{gs}			10.3		
Gate-drain charge	Q_{gd}			4.2		
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 15\text{ V}, I_D = 40\text{ A}, V_{GS} = 10\text{ V},$ $R_{GEN} = 1.6\text{ }\Omega$		6.0		ns
Rise time	t_r			3.7		
Turn-off delay time	$t_{d(off)}$			23.1		
Fall time	t_f			5.6		
Input capacitance	C_{iss}	$V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		3931		pF
Output capacitance	C_{oss}			925		
Reverse transfer capacitance	C_{rss}			37		
Reverse Diode Characteristics ⁽⁵⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_F = 40\text{ A}$		0.8	1.1	V
Reverse recovery time	t_{rr}	$V_{DS} = 15\text{ V}, I_F = 40\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		38		ns
Reverse recovery charge	Q_{rr}			34		nC

Notes

(5) Guaranteed by design, not subject to production testing.

5. Q1 Electrical characteristics diagrams

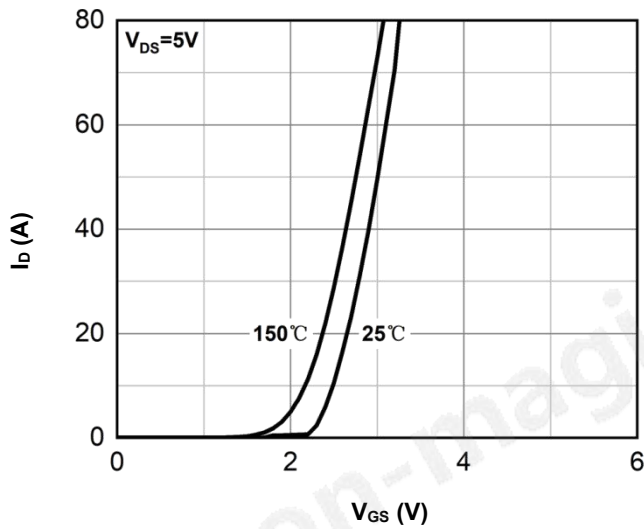
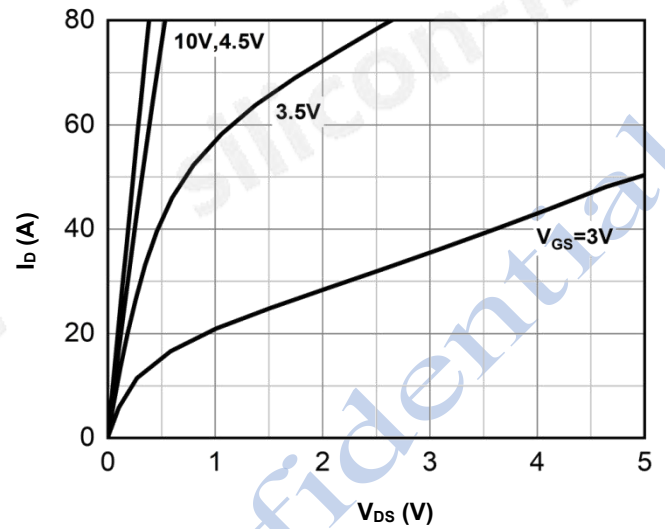
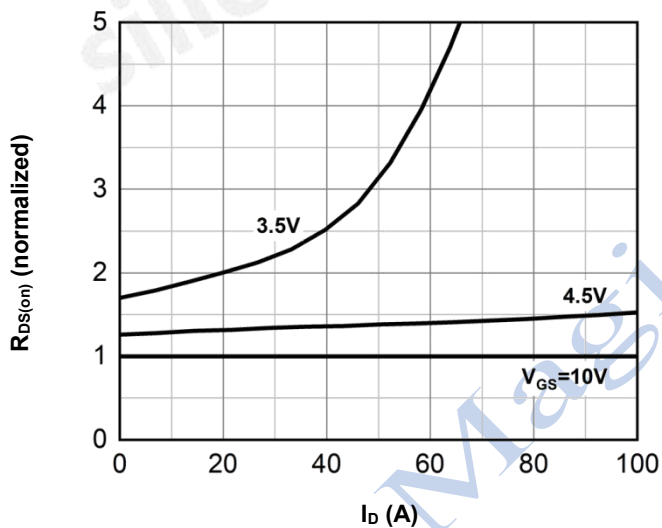
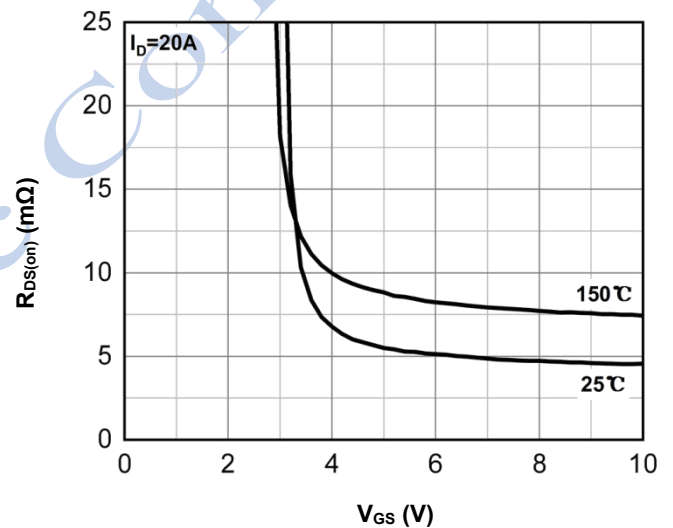
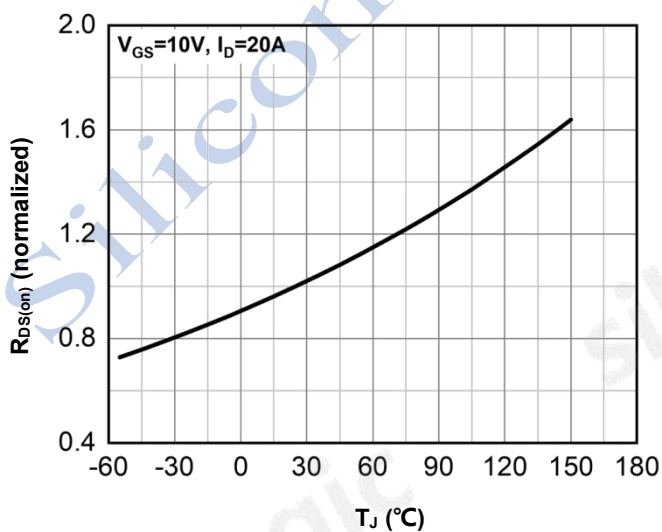
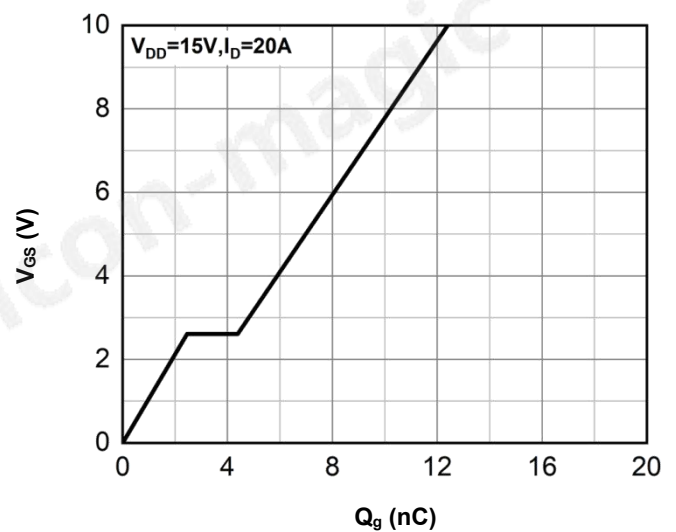
Fig.1 Typ. transfer characteristics

Fig.2 Typ. output characteristics

Fig.3 Normalized on-resistance vs drain current

Fig.4 Typ. on-resistance vs gate-source voltage

Fig.5 Normalized on-resistance vs junction temperature

Fig.6 Typ. gate charge


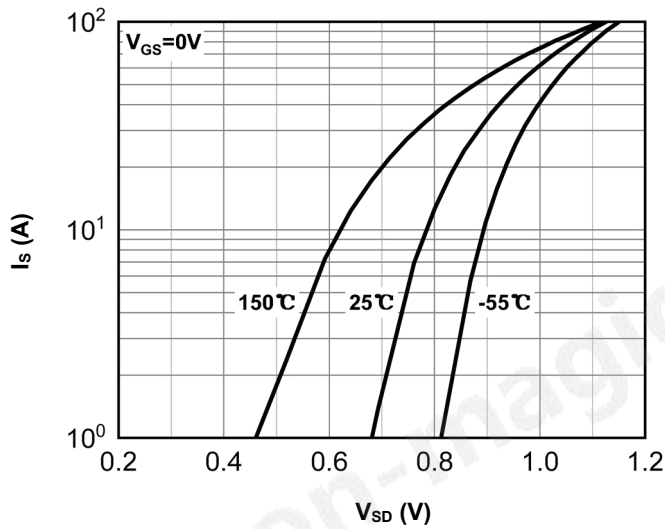
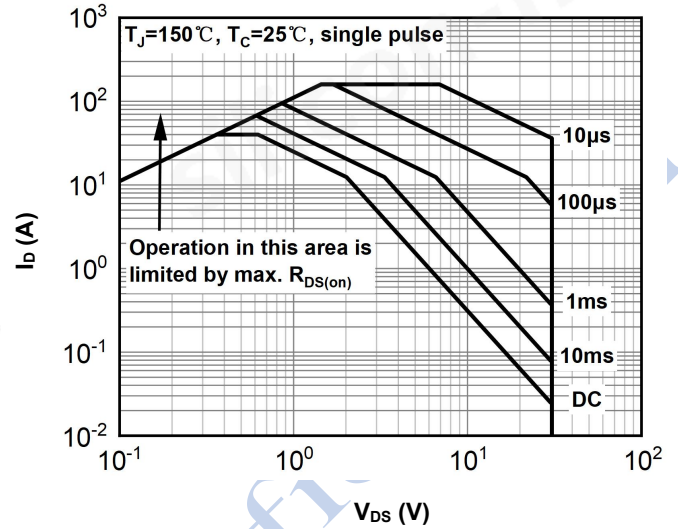
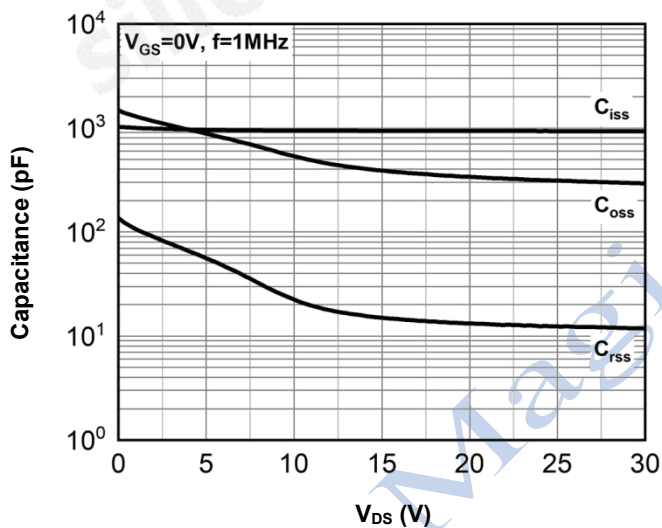
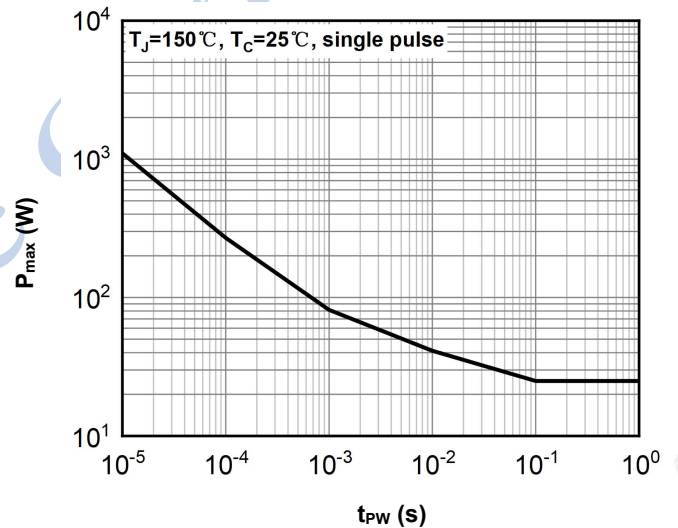
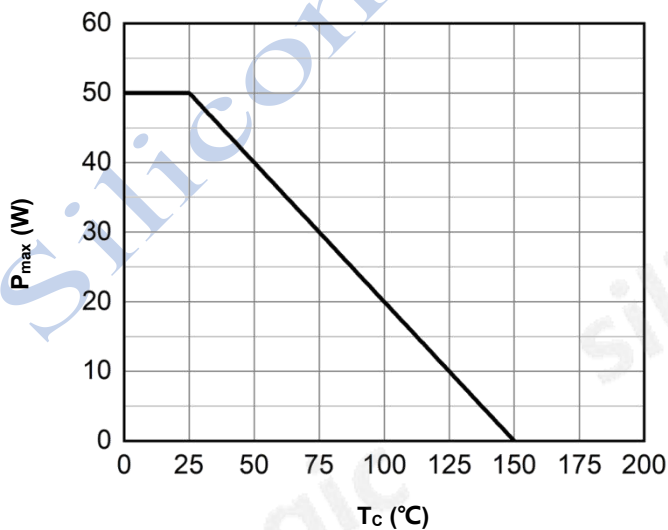
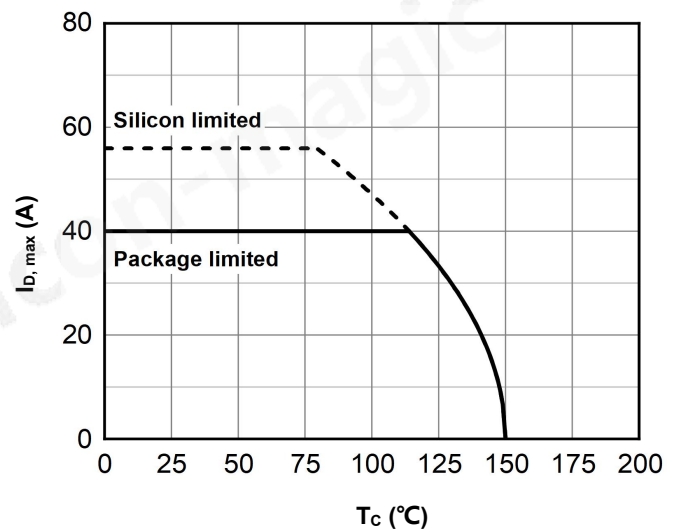
Fig.7 Typ. forward characteristics of body diode

Fig.8 Safe operating area

Fig.9 Typ. Capacitance

Fig.10 Single pulse maximum power dissipation

Fig.11 Max. power dissipation vs case temperature

Fig.12 Max. continuous drain current vs case temperature


Fig.13 Normalized $V_{(BR)DSS}$ vs junction temperature

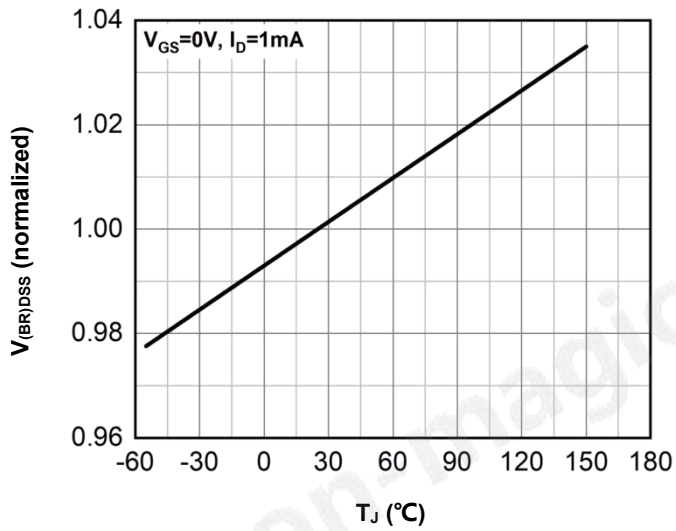


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

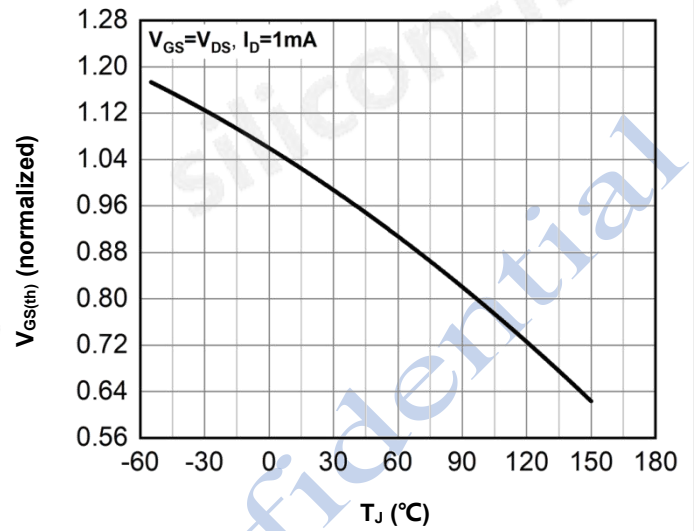
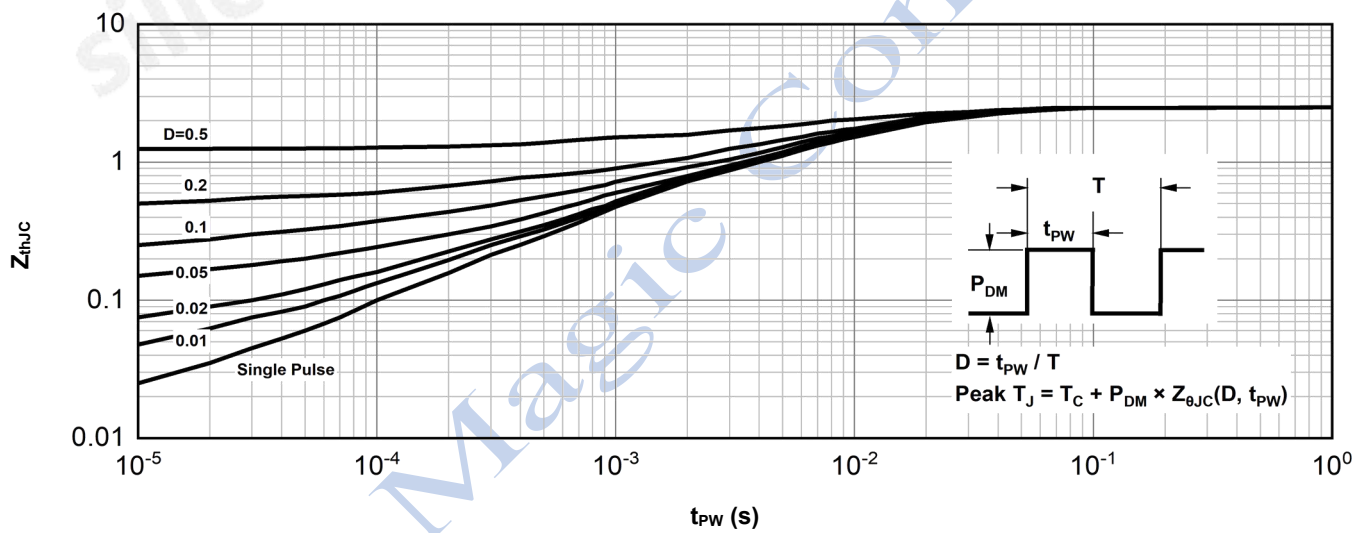


Fig.15 Transient thermal impedance from junction to case



6. Q2 Electrical characteristics diagrams

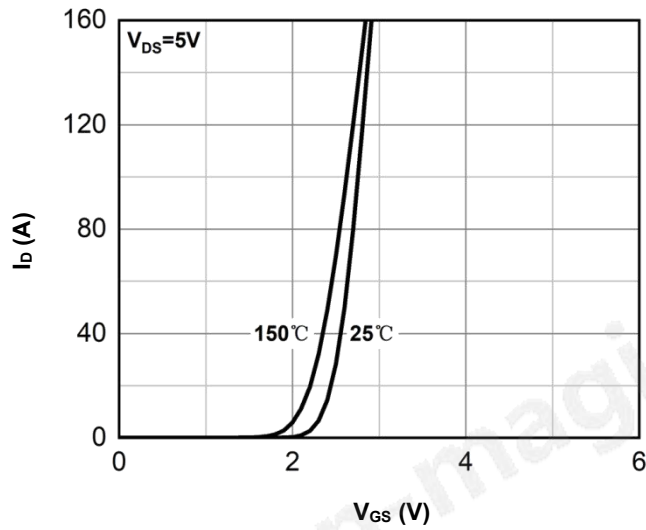
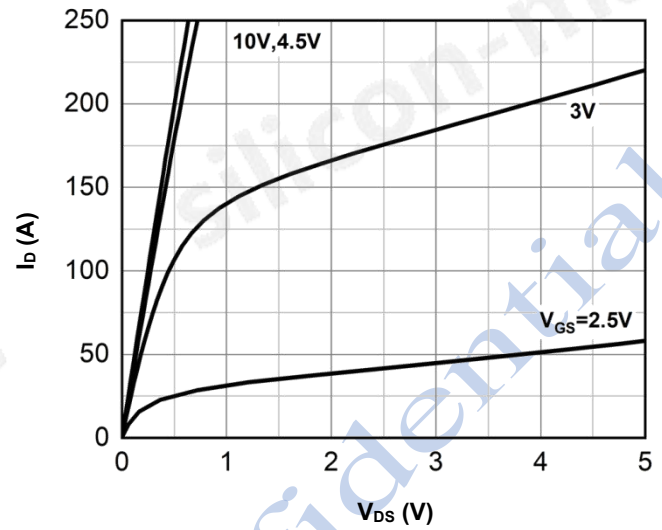
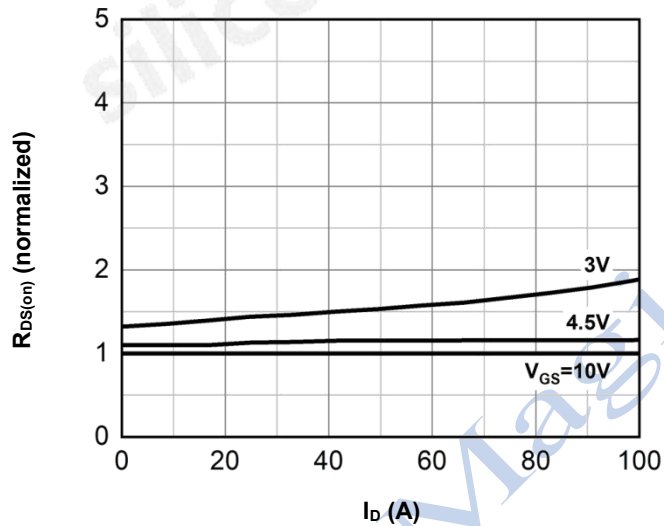
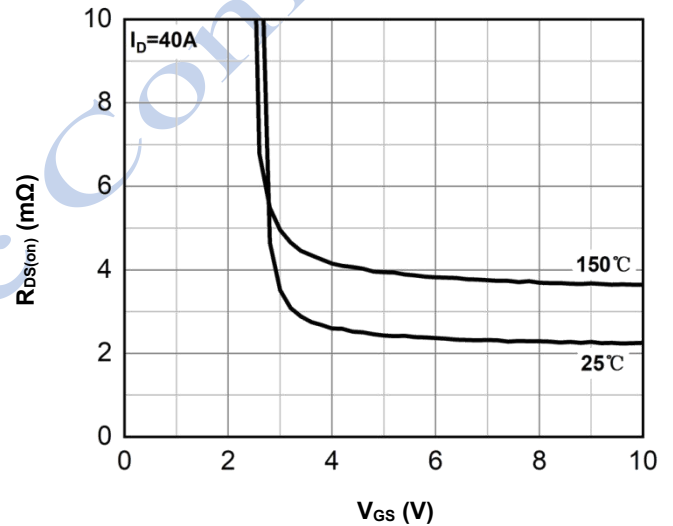
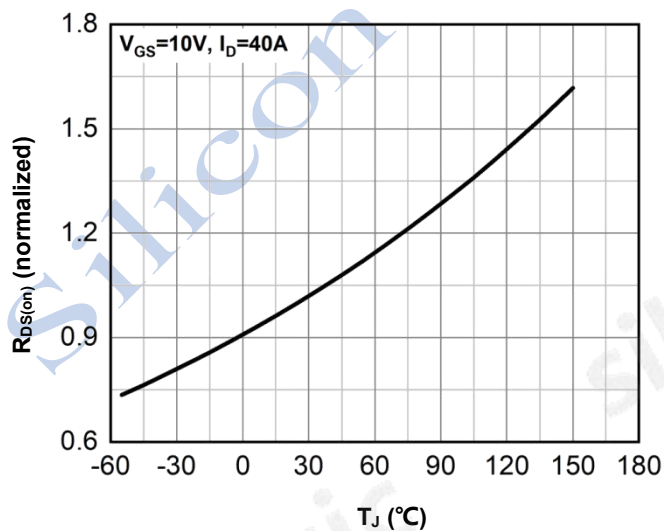
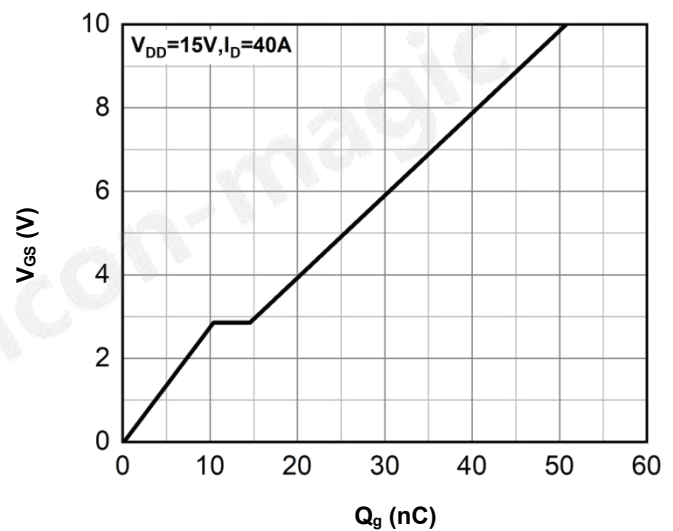
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Fig.2 Typ. output characteristics

Fig.3 Normalized on-resistance vs drain current

Fig.4 Typ. on-resistance vs gate-source voltage

Fig.5 Normalized on-resistance vs junction temperature

Fig.6 Typ. gate charge


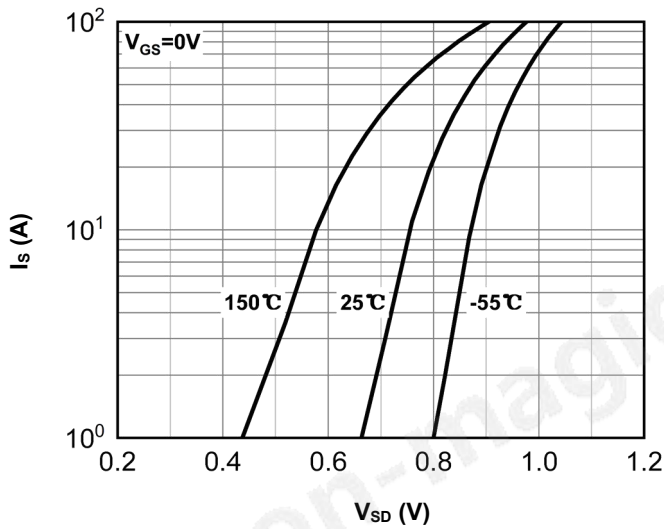
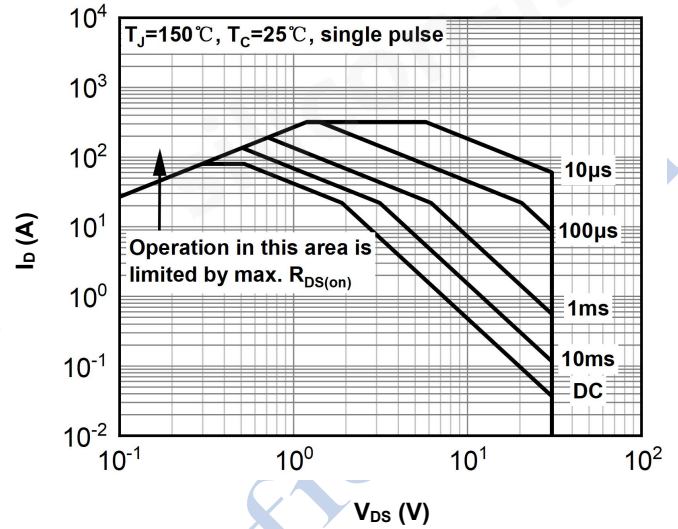
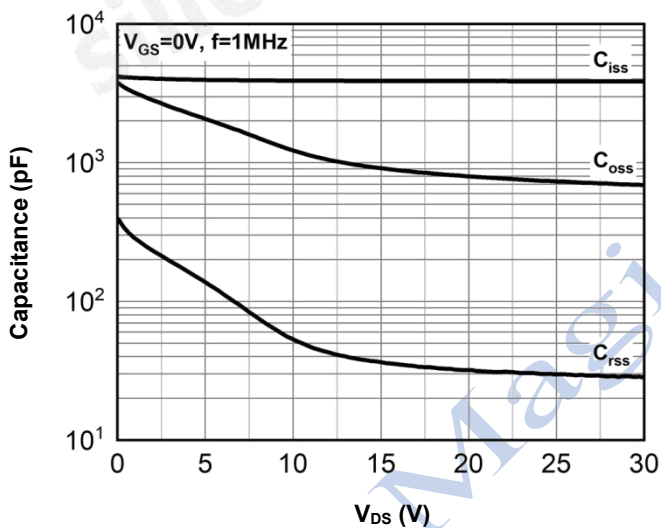
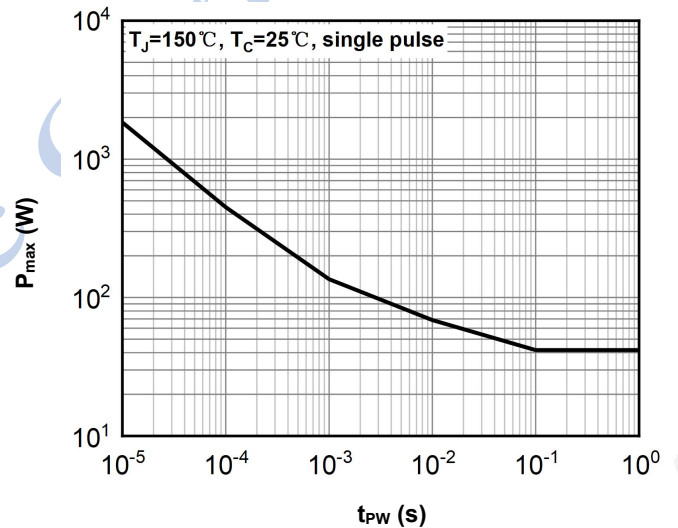
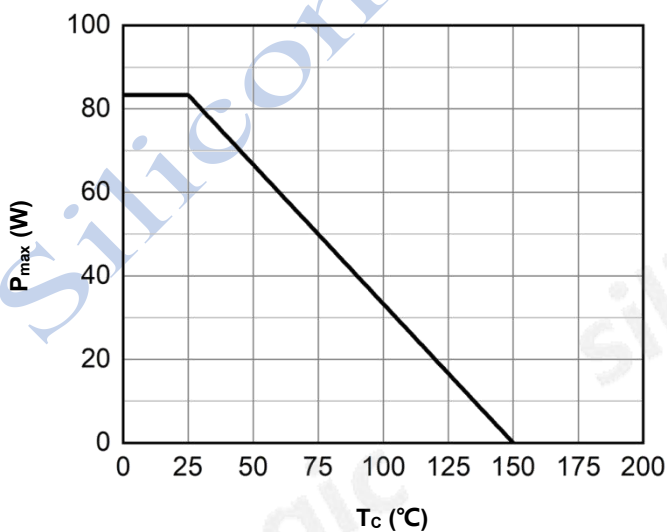
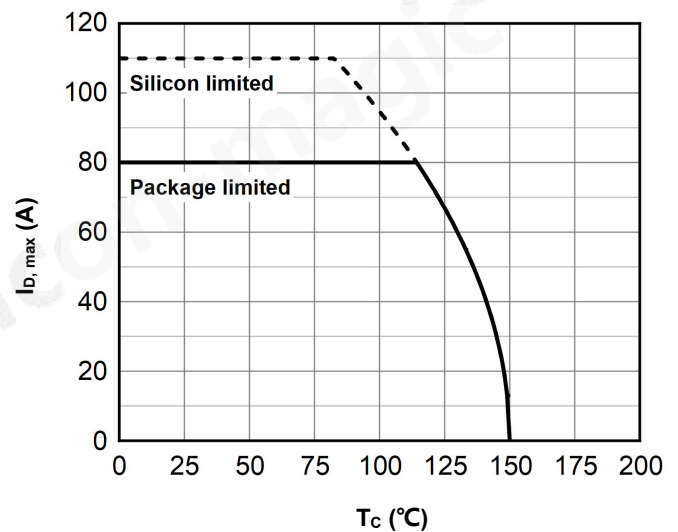
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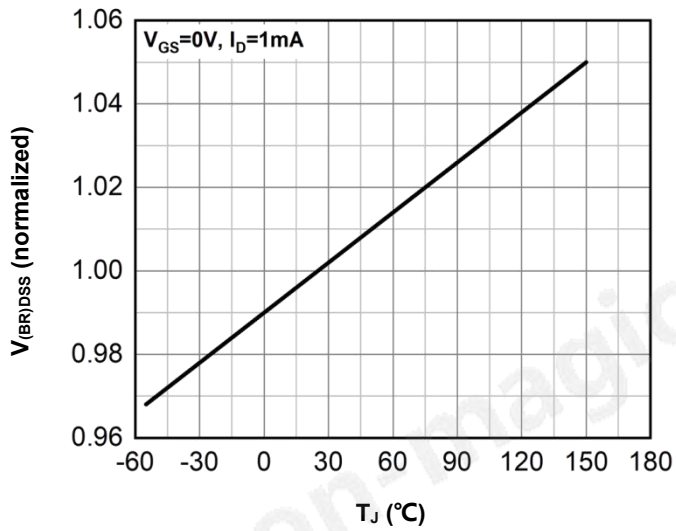


Fig.14 Normalized $V_{GS(th)}$ vs junction temperature

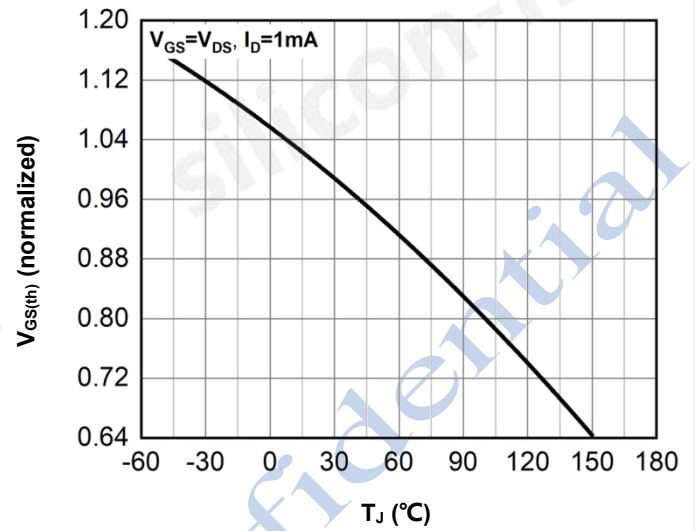
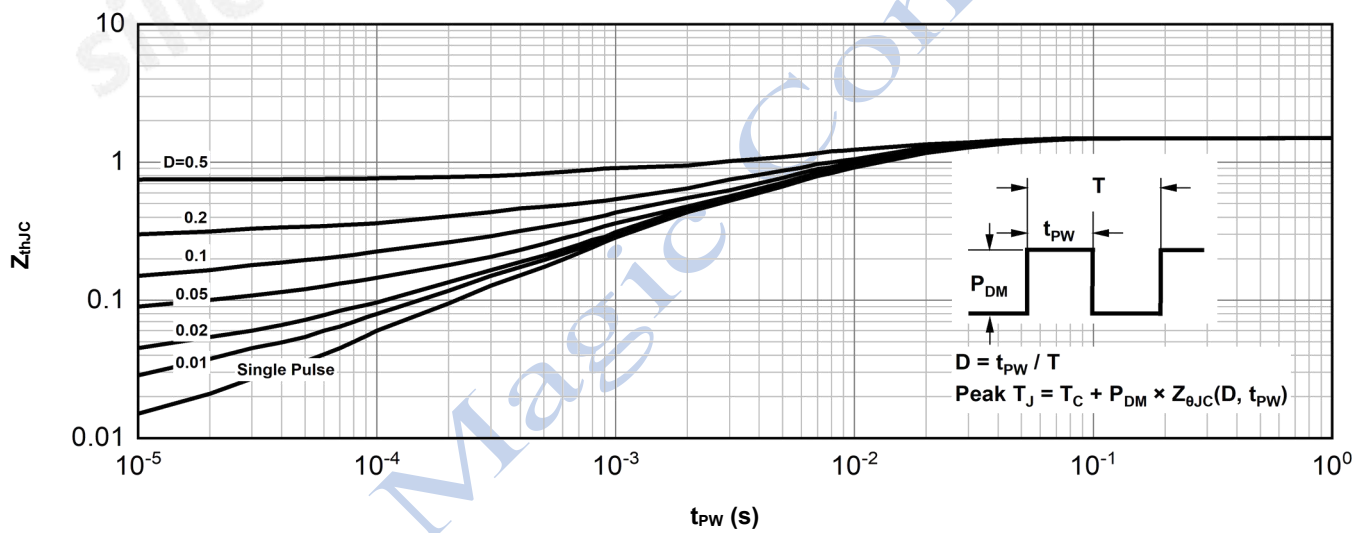
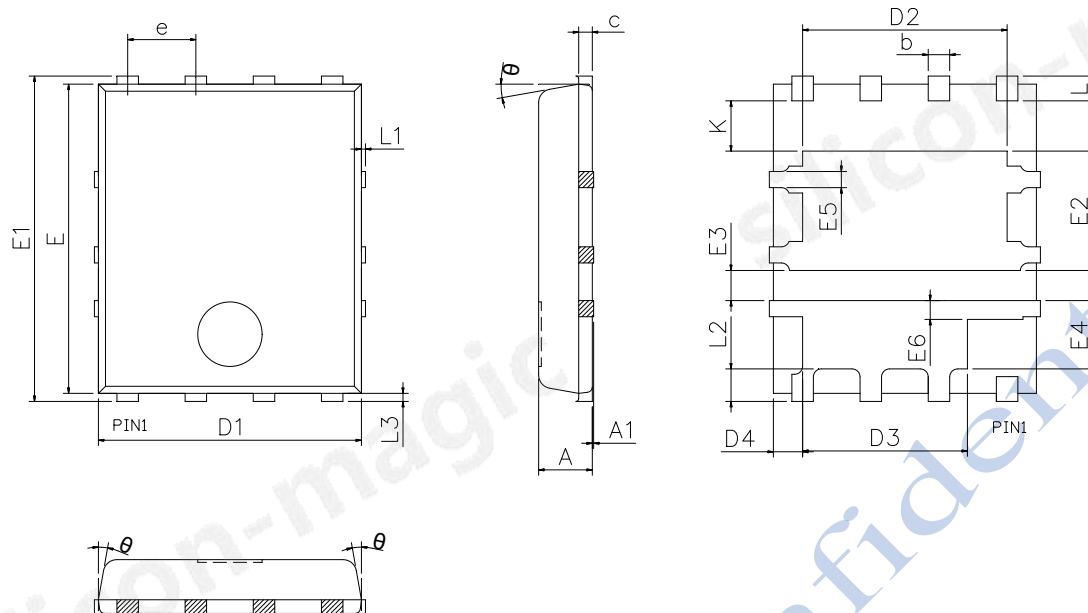


Fig.15 Transient thermal impedance from junction to case



7. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	0.90	1.00	1.10
A1	0.00	—	0.05
b	0.33	0.40	0.51
c	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
D3	2.87	3.07	3.22
D4	0.45	0.55	0.65
E	5.70	5.75	5.80
E1	5.90	6.05	6.15
E2	2.02	2.22	2.32
E3	0.45	0.55	0.65
E4	1.22	1.32	1.42
E5	0.20	—	0.40
E6	0.31	—	0.51
e	1.27		
L	0.39	0.46	0.61
L1	0.00	—	0.20
L2	0.48	0.58	0.68
L3	0.06	0.15	0.25
K	0.70	0.95	1.20
θ	0°	10°	12°

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