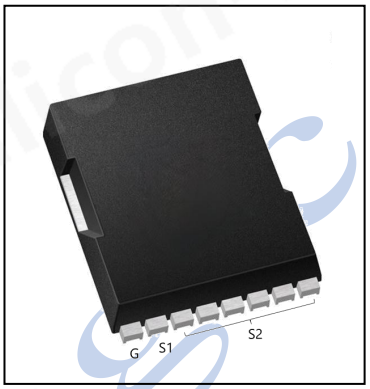
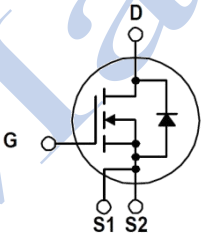
N-Channel 650V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (mΩ)	I_D (A)
650	70 @ V_{GS} = 10V	47 (1)

TOLL2





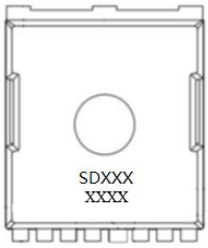
Pb-free
RoHS COMPLIANT
HALOGEN FREE

Features

- Low $R_{DS(on)}$ and FOM
- Low Switching loss
- 100% avalanche tested. High avalanche ruggedness
- Ultra-fast and robust body diode

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar



SDXXX
Device code
Silicon Magic discrete device
XXXX
Wafer lot number
Work week code
Year code

Package and ordering information

Ordering code	Package	Device code
SDH65N070QF-AA	TOLL2	AOF

1. Maximum ratings

Absolute maximum ratings (T_A = 25℃ unless otherwise noted)				
Parameter		**Symbol**	**Limit**	**Unit**
Drain-source voltage		V_{DS}	650	V
Gate-source voltage		V_{GS}	±30	V
Continuous drain current(1)	T_C=25℃(1)	I_D	47	A
	T_C=100℃ (1)		30	
Pulsed drain current(2)		$I_{D,pulse}$	188	
Avalanche energy, single pulse(3)		E_{AS}	810	mJ
Power dissipation	T_C=25℃	P_D	357	W
Operating junction and storage temperature range		T_J, T_{stg}	-55 to 150	℃

2. Thermal resistance ratings

Thermal resistance ratings				
Parameter[4]		**Symbol**	**Max.**	**Unit**
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.35	°C/W
Thermal resistance, junction-to-ambient	Steady state	$R_{\theta JA}$	40	

3. Electrical characteristics

Electrical characteristics						
Parameter	**Symbol**	**Test conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 10 mA	650			V
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	3	4	5	V
Gate-body leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ±30 V			±100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 650 V, V_{GS} = 0 V			10	μA
Drain-source on-resistance	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 17 A		60	70	mΩ
Gate resistance	R_g	f = 1 MHz, open drain		1		Ω
Dynamic[4]						
Total gate charge	Q_g	V_{DS} = 400 V, I_D = 17A, V_{GS} = 10 V		76.3		nC
Gate-source charge	Q_{gs}			22		
Gate-drain charge	Q_{gd}			24		
Turn-on delay time	$t_{d(on)}$	V_{DS} = 400 V, I_D = 17 A, V_{GS} = 10 V, R_{GEN} = 6.8 Ω		48.5		ns
Rise time	t_r			13		
Turn-off delay time	$t_{d(off)}$			75.3		
Fall time	t_f			5		
Input capacitance	C_{iss}	V_{DS} = 400 V, V_{GS} = 0 V, f = 100 KHz		4096		pF
Output capacitance	C_{oss}			84		
Reverse transfer capacitance	C_{rss}			5		
Energy related output capacitance	$C_{oss(er.)}$	V_{DS} = 0 V to 400 V, V_{GS} = 0 V		127		
Reverse Diode Characteristics[4]						
Diode forward voltage	V_{SD}	V_{GS} = 0 V, I_F = 34 A		0.87	1.1	V
Reverse recovery time	t_{rr}	V_{DS} = 400 V,I_F = 17 A, di/dt = 100 A/μs		128		ns
Reverse recovery charge	Q_{rr}			664		nC

Notes

(1) Limited by maximum junction temperature.

(2) Pulse width limited by maximum junction temperature.

(3) V_{DS} = 130 V, V_{GS} = 10 V, L = 60 mH.

(4) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

Fig.1 Typ. transfer characteristics

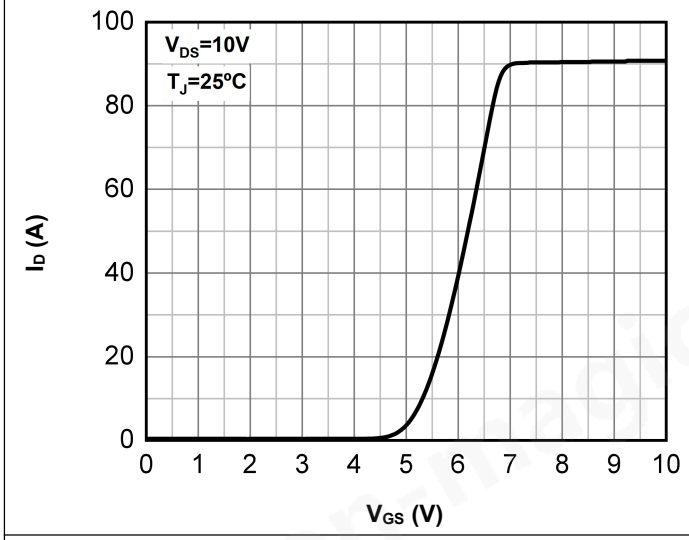


Fig.2 Typ. output characteristics at 25℃

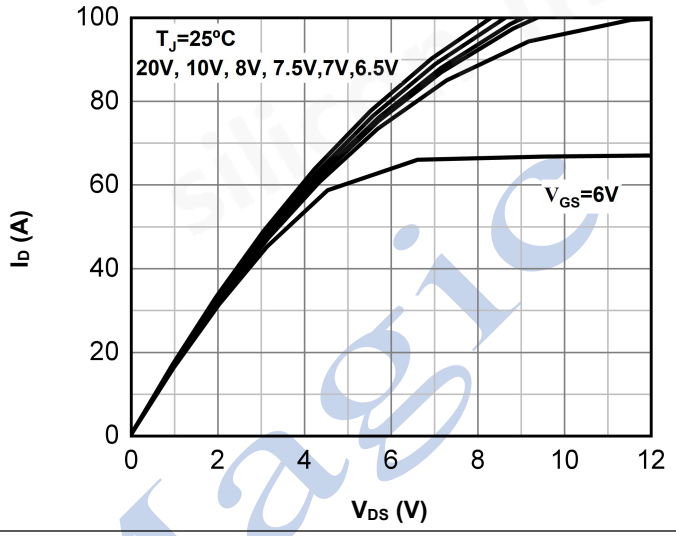


Fig.3 Normalized on-resistance vs junction temperature

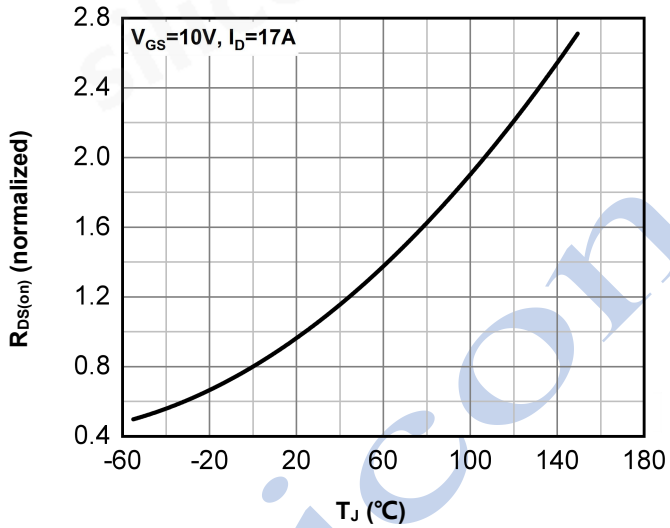


Fig.4 Normalized on-resistance vs drain current

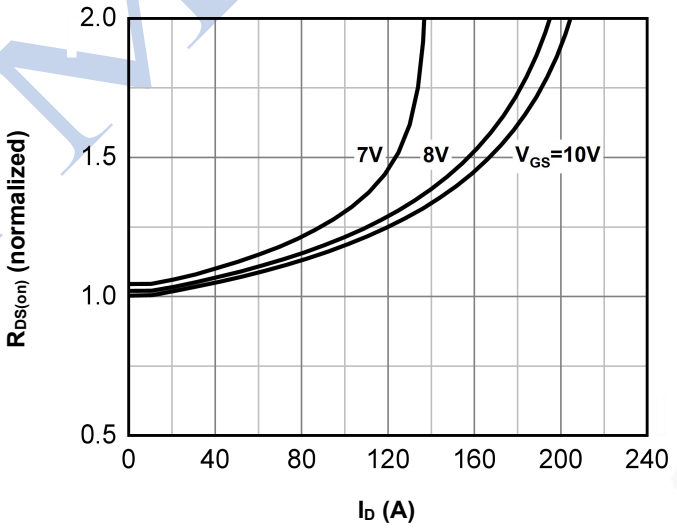


Fig.5 Typ. capacitance

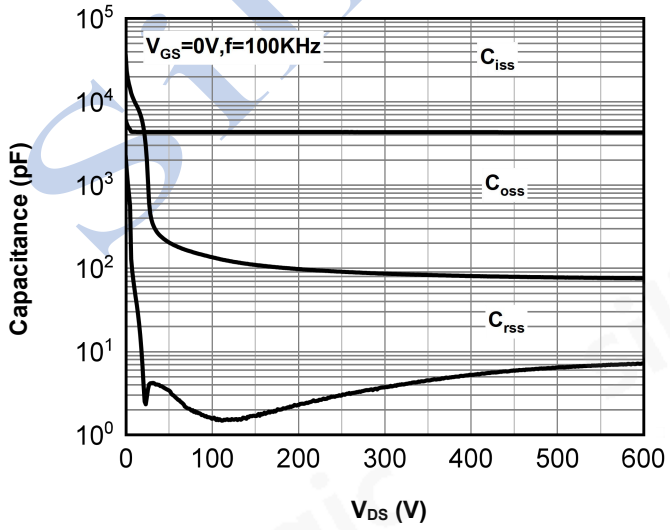


Fig.6 Typ. gate charge

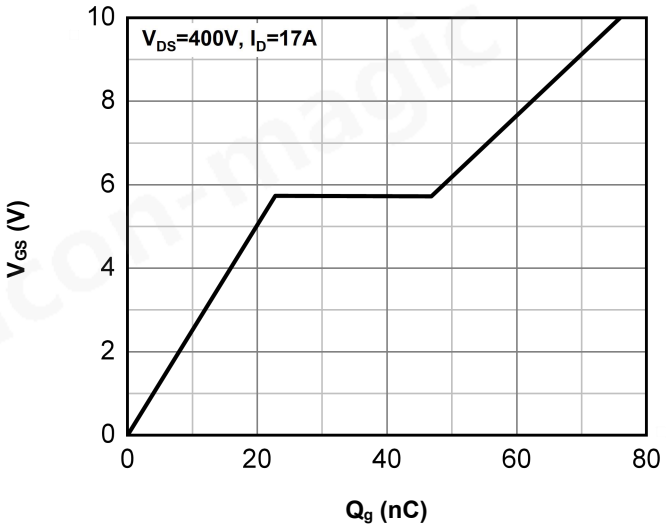


Fig.7 Typ. forward characteristics of body diode

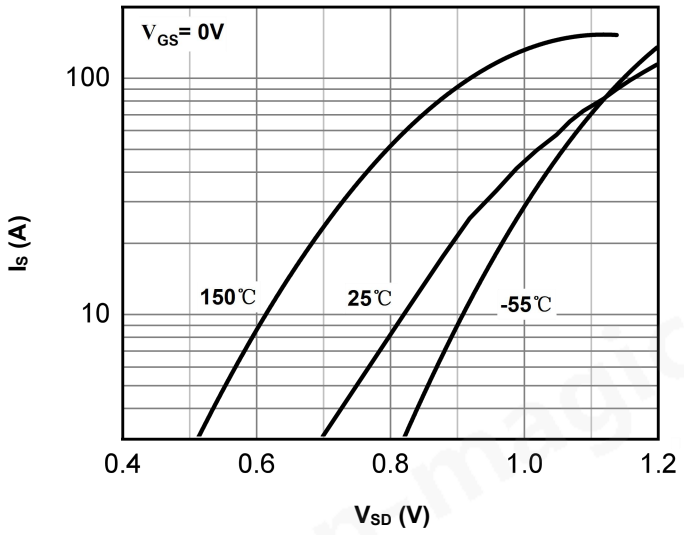


Fig.8 Safe operating area

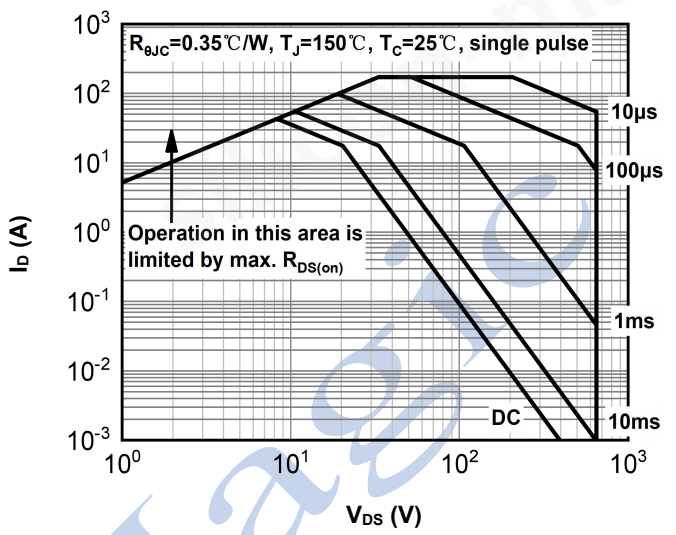


Fig.9 Drain current vs case temperature

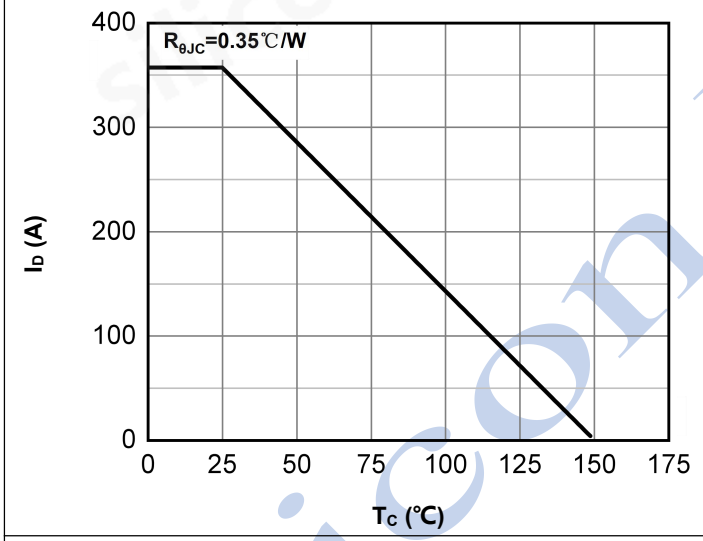


Fig.10 Typ. C_{oss} stored energy

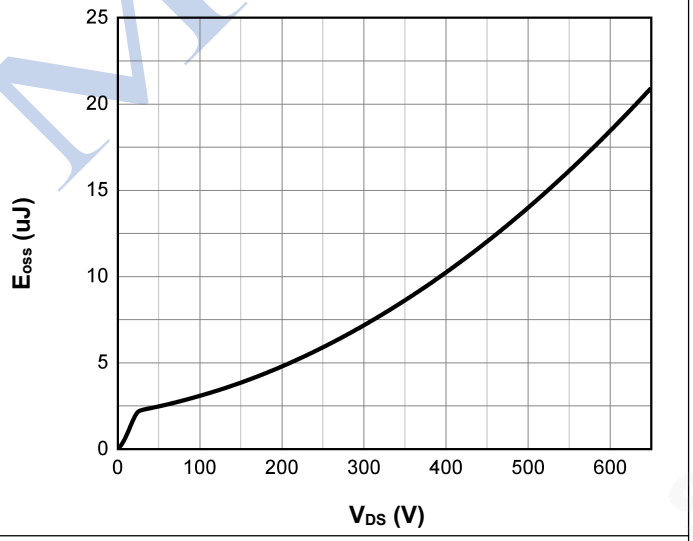


Fig.11 Normalized $V_{(BR)DSS}$ vs junction temperature

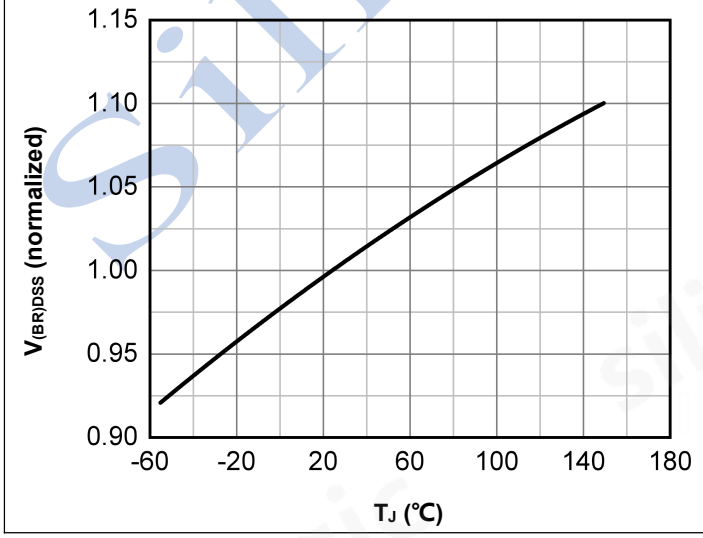


Fig.12 Normalized $V_{GS(th)}$ vs junction temperature

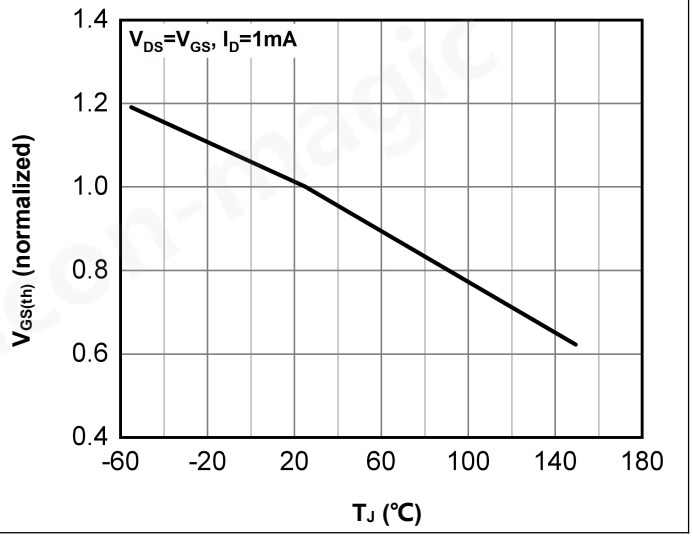
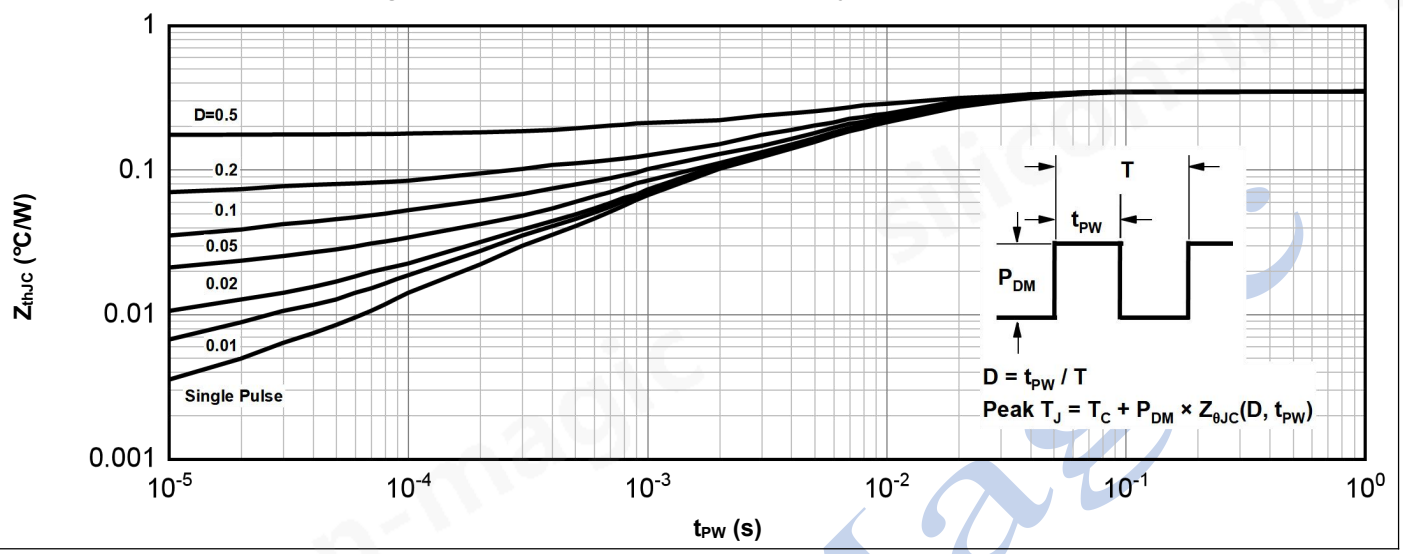


Fig.13 Transient thermal impedance from junction to case



5. Test circuits and waveforms

Figure 14. Gate charge test circuit & waveforms

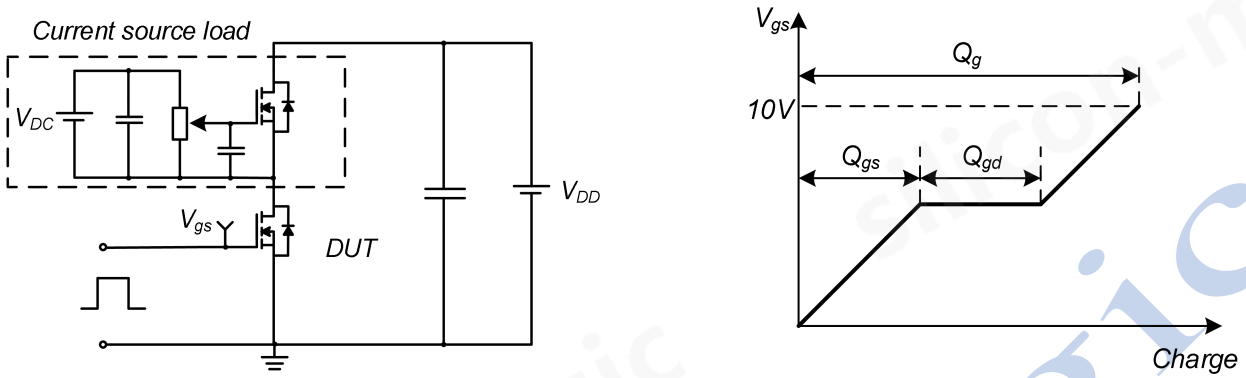


Figure 15. Switching time test circuit & waveforms

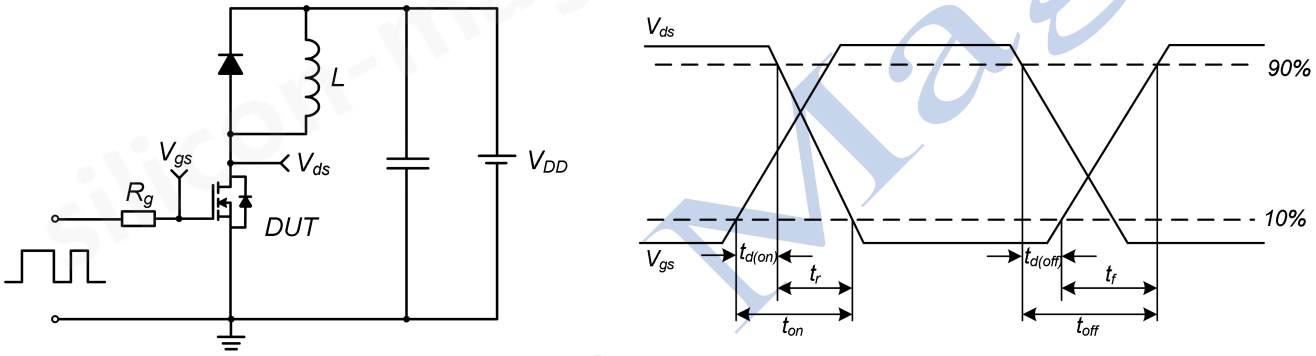


Figure 16. Diode reverse recovery test circuit & waveforms

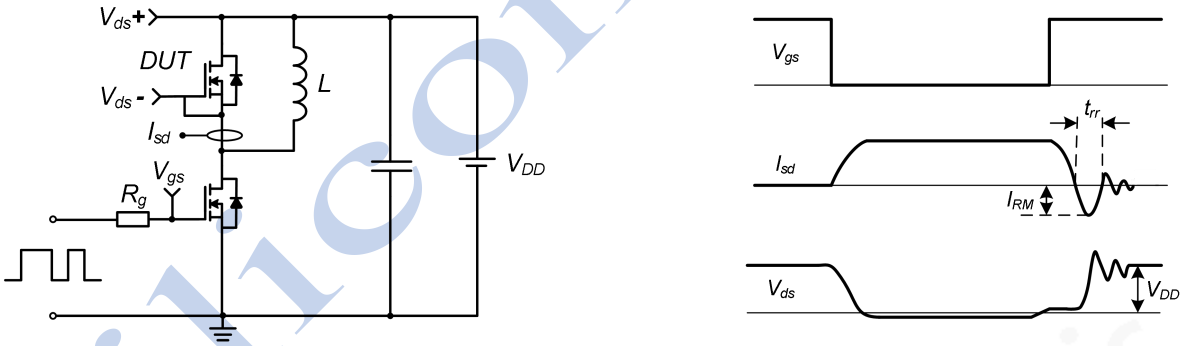
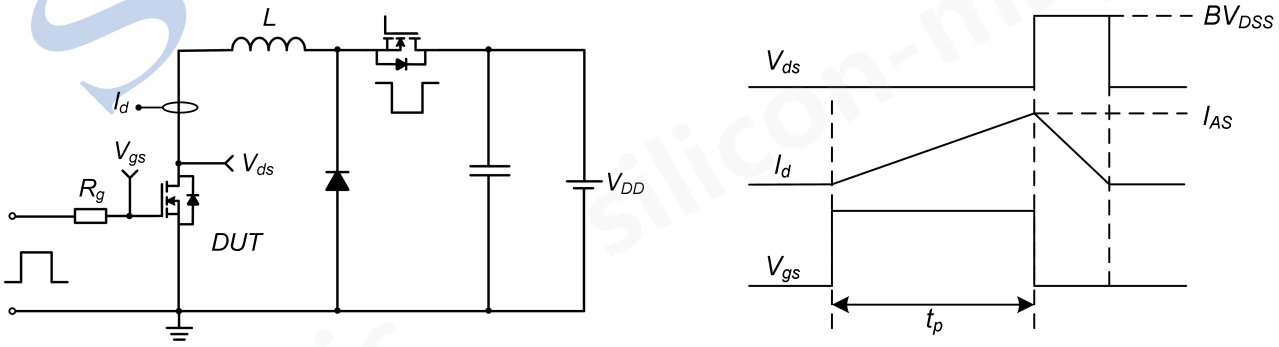
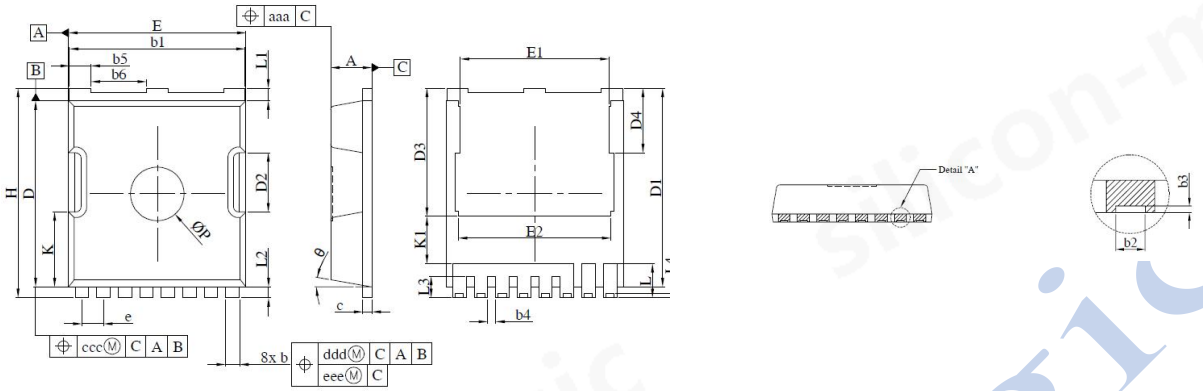


Figure 17. Unclamped inductive switching test circuit & waveforms



6. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	2.20	2.30	2.40
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.36	0.45	0.55
b3	0.05	0.10	0.35
b4	0.30	0.40	0.50
b5	1.10	1.20	1.30
b6	3.00	3.10	3.20
c	0.40	0.50	0.60
D	10.28	10.38	10.55
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	7.00	7.15	7.30
D4	3.44	3.59	3.74
e	1.10	1.20	1.30
E	9.80	9.90	10.00
E1	8.20	8.30	8.40
E2	8.35	8.50	8.65
H	11.50	11.68	11.85
K	4.08	4.18	4.28
K1	2.45	-	-
L	1.60	1.90	2.10
L1	0.50	0.70	0.90
L2	0.50	0.60	0.70
L3	1.00	1.20	1.30
L4	0.13	0.23	0.33
P	2.85	3.00	3.15
θ	10° REF		
aaa	0.20		
ccc	0.20		
ddd	0.25		
eee	0.20		

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