

N-Channel 650V MOSFET

Product summary

V_{DS} (V)	$R_{DS(on),max}$ (m Ω)	I_D (A)
650	70 @ $V_{GS} = 10V$	47 ⁽¹⁾

Features

- Low $R_{DS(on)}$ and FOM
- Low Switching loss
- 100% avalanche tested. High avalanche ruggedness
- Ultra-fast and robust body diode

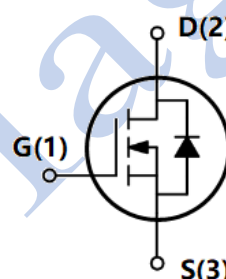
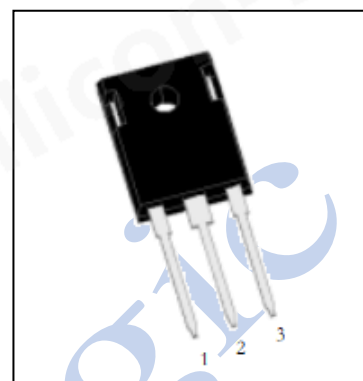
Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- EV Charger
- UPS / Solar

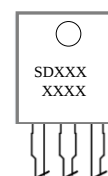
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Package and ordering information

Ordering code	Package	Device code
SDH65N070WF-AA	TO247-3L	AQF

TO247-3L


RoHS
COMPLIANT
HALOGEN
FREE



SDXXX
XXXX

Device code
Silicon Magic discrete device

XXXX
Wafer lot number
Work week code
Year code

1. Maximum ratings

Absolute maximum ratings ($T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source voltage	V_{DS}	650	V
Gate-source voltage	V_{GS}	± 30	V
Continuous drain current ⁽¹⁾	$T_C=25^\circ\text{C}^{(1)}$	I_D 47	A
	$T_C=100^\circ\text{C}^{(1)}$	30	
Pulsed drain current ⁽²⁾	$I_{D,pulse}$	188	
Avalanche energy, single pulse ⁽³⁾	E_{AS}	810	mJ
Power dissipation	$T_C=25^\circ\text{C}$	P_D 357	W
Operating junction and storage temperature range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

2. Thermal resistance ratings

Thermal resistance ratings						
Parameter ⁽⁴⁾		Symbol	Max.	Unit		
Thermal resistance, junction-to-case	Steady state	$R_{\theta JC}$	0.35	°C/W		
Thermal resistance, junction-to-ambient	Steady state	$R_{\theta JA}$	40			

3. Electrical characteristics

Electrical characteristics						
Parameter	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Static parameter						
Drain to source breakdown voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 10\text{ mA}$	650			V
Gate-source threshold voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 1\text{ mA}$	3	4	5	V
Gate-body leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 30\text{ V}$			±100	nA
Zero gate voltage drain current	I_{DSS}	$V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$			10	μA
Drain-source on-resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$		60	70	mΩ
Gate resistance	R_g	$f = 1\text{ MHz}, \text{open drain}$		0.9		Ω
Dynamic ⁽⁴⁾						
Total gate charge	Q_g	$V_{DS} = 400\text{ V}, I_D = 17\text{ A}, V_{GS} = 10\text{ V}$		76.3		nC
Gate-source charge	Q_{gs}			22		
Gate-drain charge	Q_{gd}			25.7		
Turn-on delay time	$t_{d(on)}$	$V_{DS} = 400\text{ V}, I_D = 17\text{ A}, V_{GS} = 10\text{ V},$ $R_{GEN} = 6.8\text{ }\Omega$		48.5		ns
Rise time	t_r			13		
Turn-off delay time	$t_{d(off)}$			75.3		
Fall time	t_f			5		
Input capacitance	C_{iss}	$V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, f = 100\text{ KHz}$		4096		pF
Output capacitance	C_{oss}			84		
Reverse transfer capacitance	C_{rss}			8		
Energy related output capacitance	$C_{oss(er.)}$	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$		127		
Reverse Diode Characteristics ⁽⁴⁾						
Diode forward voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_F = 34\text{ A}$		0.87	1.1	V
Reverse recovery time	t_{rr}	$V_{DS} = 400\text{ V}, I_F = 17\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		128		ns
Reverse recovery charge	Q_{rr}			664		nC

Notes

- (1) Limited by maximum junction temperature.
- (2) Pulse width limited by maximum junction temperature.
- (3) $V_{DS} = 130\text{ V}, V_{GS} = 10\text{ V}, L = 60\text{ mH}$.
- (4) Guaranteed by design, not subject to production testing.

4. Electrical characteristics diagrams

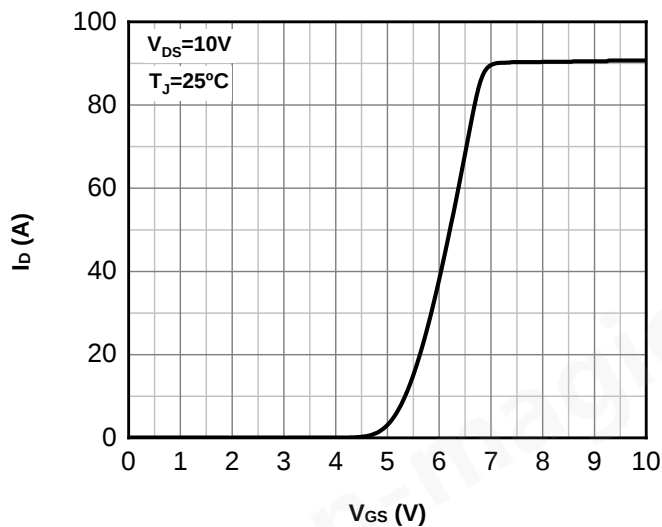
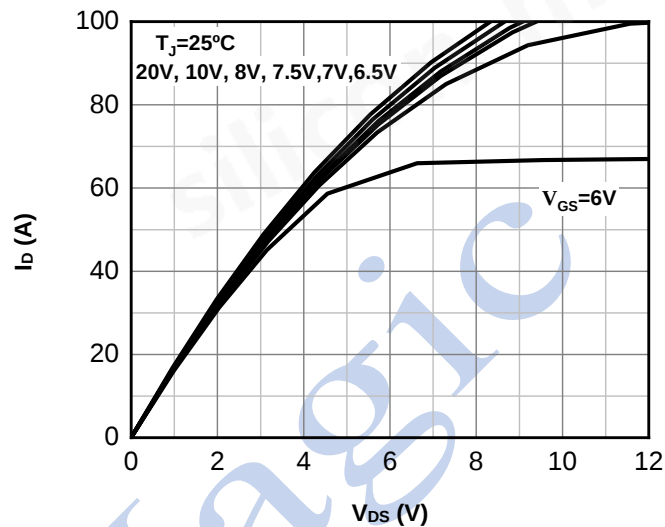
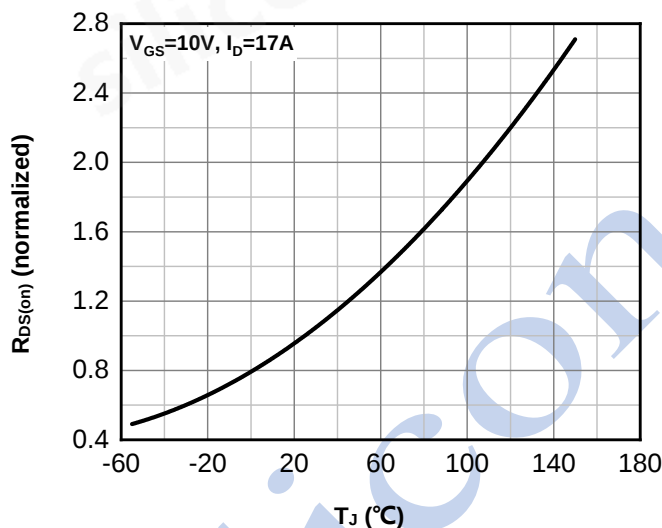
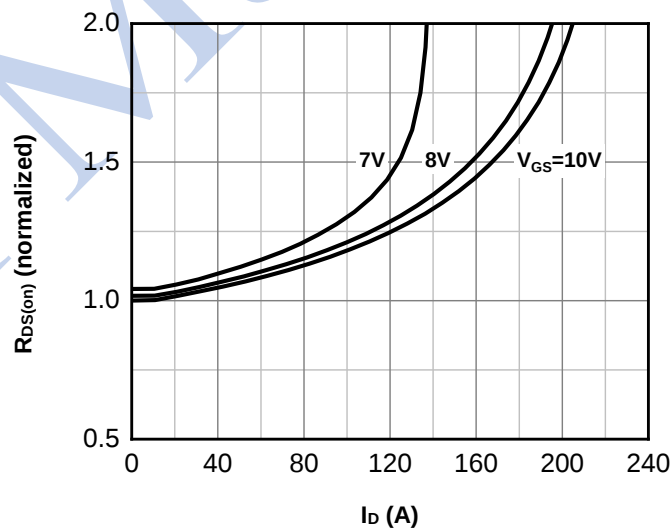
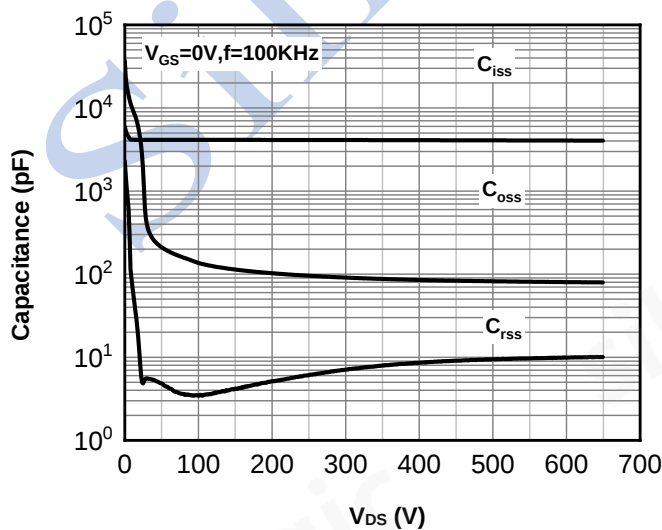
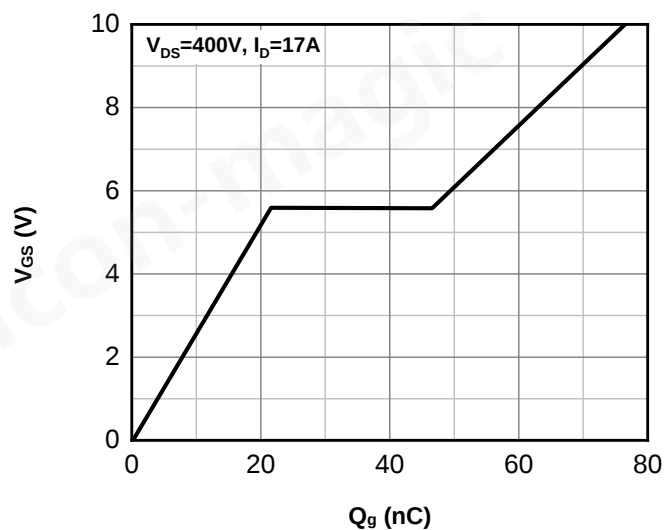
Fig.1 Typ. transfer characteristics

Fig.2 Typ. output characteristics at 25°C

Fig.3 Normalized on-resistance vs junction temperature

Fig.4 Normalized on-resistance vs drain current

Fig.5 Typ. capacitance

Fig.6 Typ. gate charge


Fig.7 Typ. forward characteristics of body diode

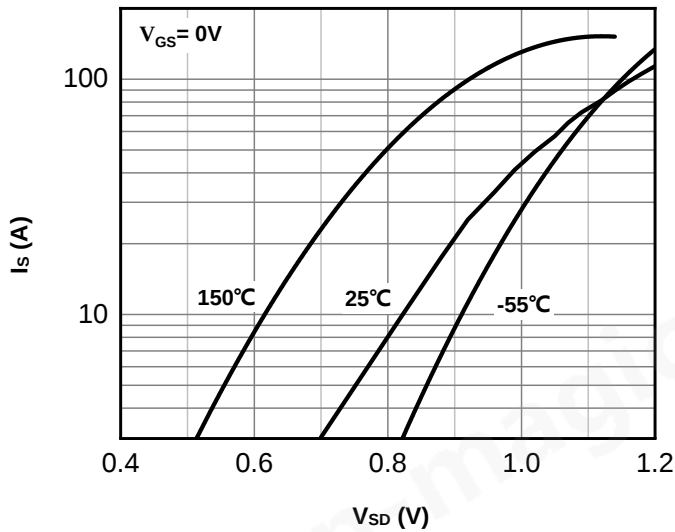


Fig.8 Safe operating area

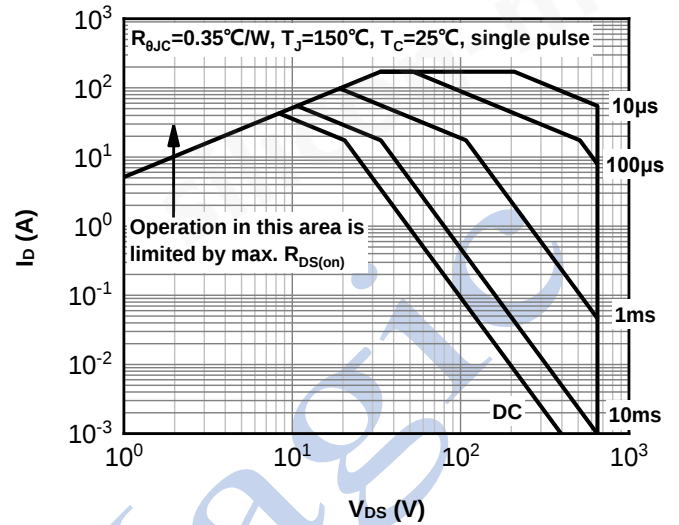


Fig.9 Drain current vs case temperature

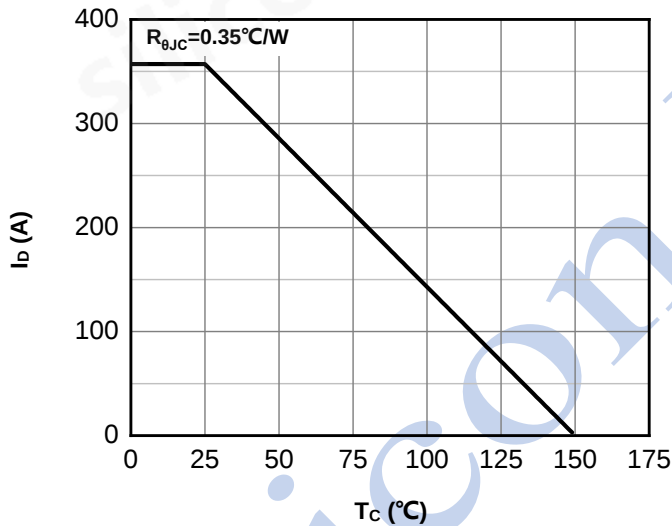


Fig.10 Typ. Coss stored energy

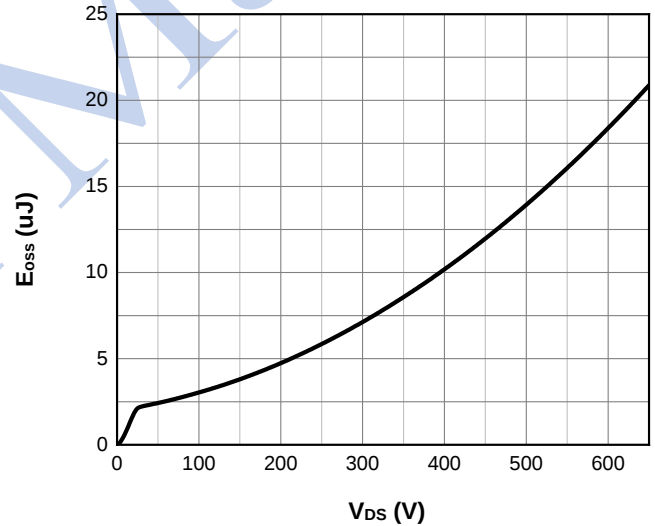


Fig.11 Normalized V(BR)DSS vs junction temperature

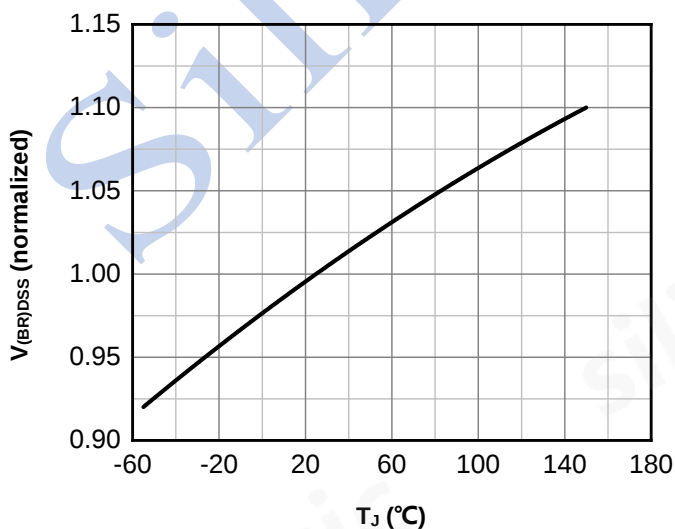
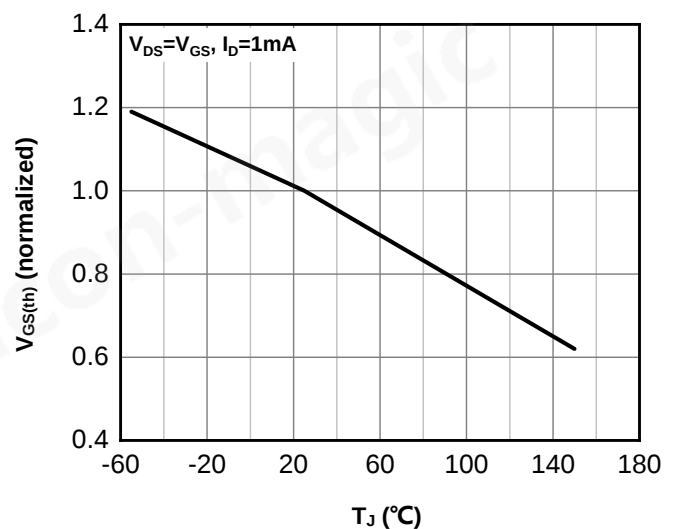
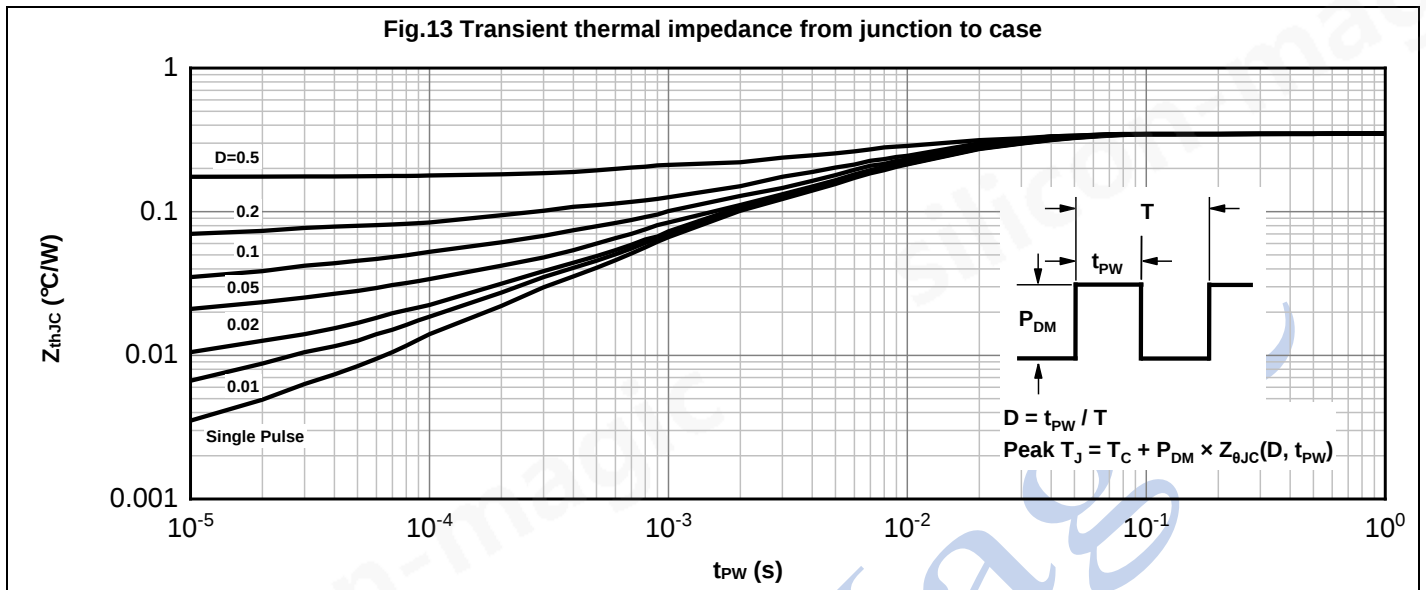


Fig.12 Normalized VGS(th) vs junction temperature





5. Test circuits and waveforms

Figure 14. Gate charge test circuit & waveforms

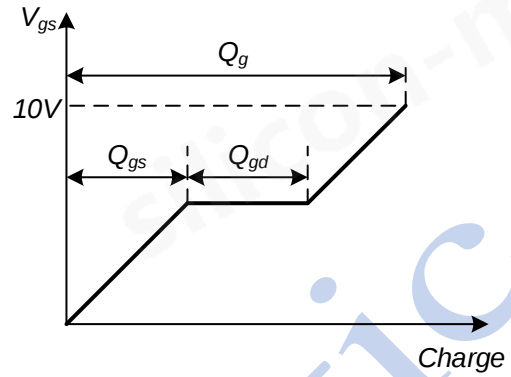
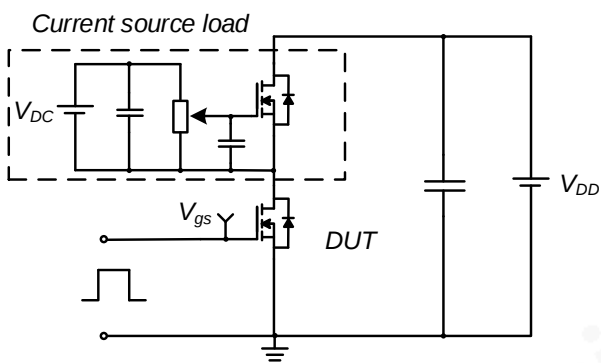


Figure 15. Switching time test circuit & waveforms

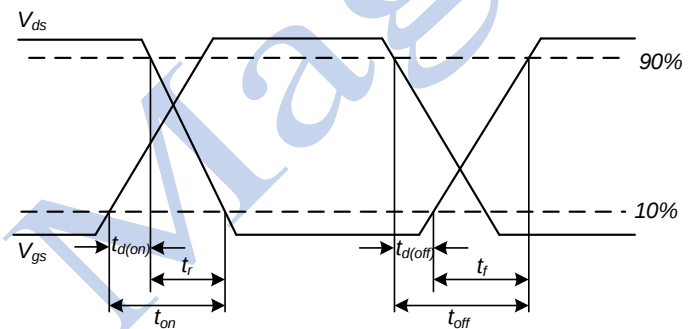
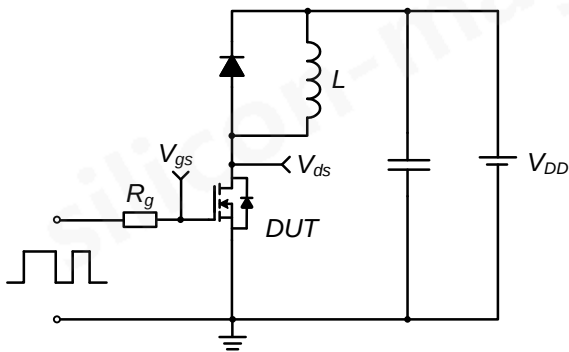


Figure 16. Diode reverse recovery test circuit & waveforms

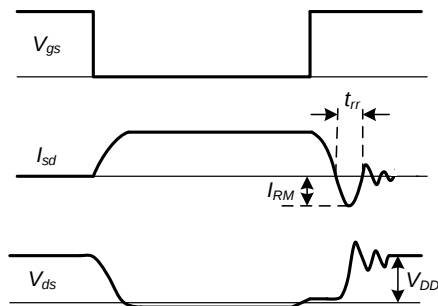
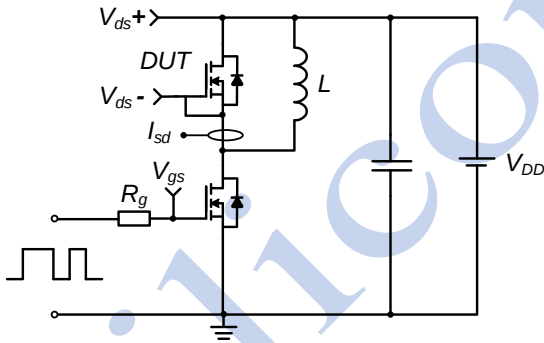
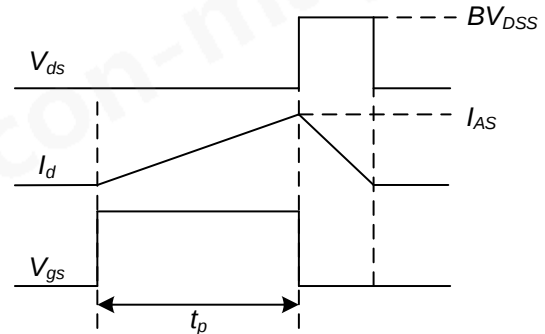
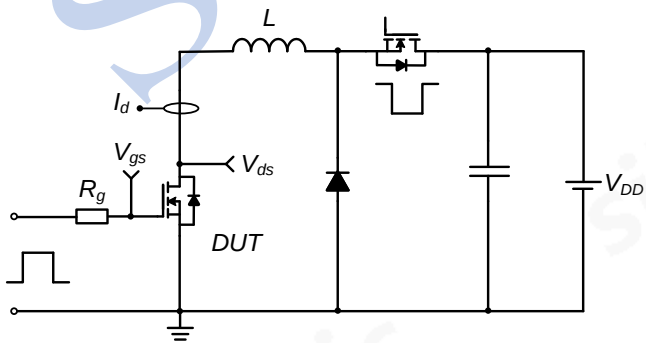
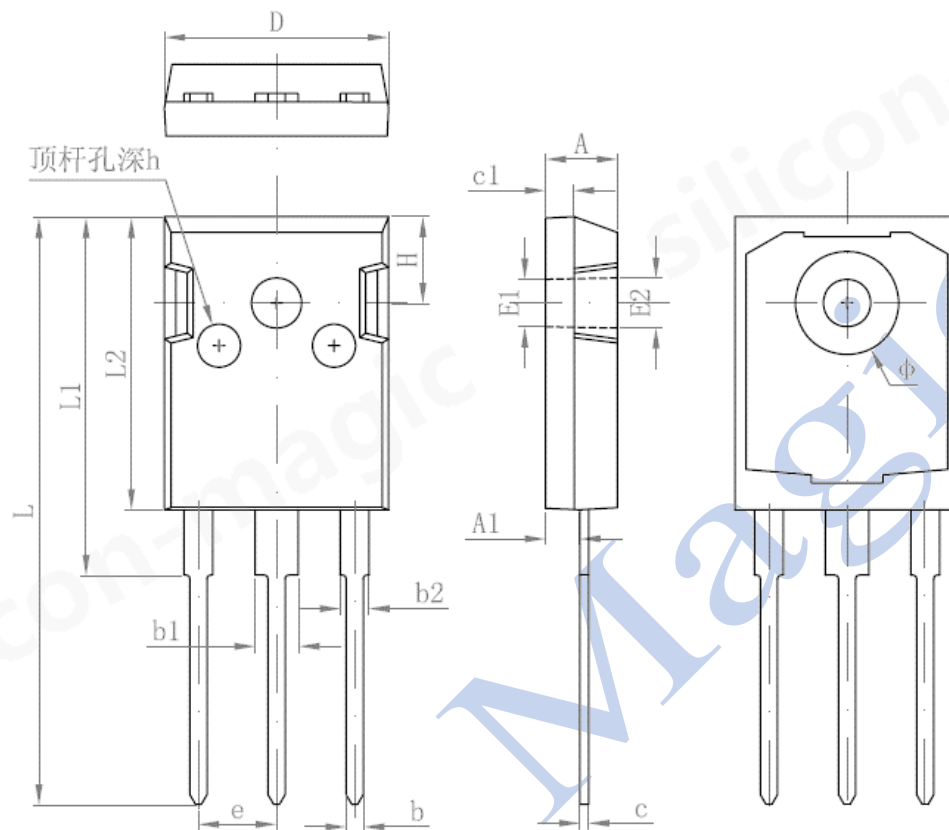


Figure 17. Unclamped inductive switching test circuit & waveforms



6. Package outline dimensions



Dim	Millimeters		
	Min	Nom	Max
A	4.850	-	5.150
A1	2.200	-	2.600
b	1.000	-	1.400
b1	2.800	-	3.200
b2	1.800	-	2.200
c	0.500	-	0.700
c1	1.900	-	2.100
D	15.450	-	15.750
E1	3.500 REF		
E2	3.600 REF		
L	40.900	-	41.300
L1	24.800	-	25.100
L2	20.300	-	20.600
Φ	7.100	-	7.300
e	5.450 TYP		
H	5.980 REF		
h	0.000	-	0.300

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